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Direct-Coupled Transistor Logic Circuitry*

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Summary—**Direct-coupled transistor logic circuitry lends itself to systematic design methods and performs remarkably well. Logical design rules are given for use with transistors which meet specifications treated in a companion paper. The implications of the use of silicon transistors are discussed.**

Introduction

THE CONCEPT of direct-coupled transistor circuitry as a sufficient system for digital computers was introduced by Beter, *et al.*,[1] in March, 1955. The present paper touches on several aspects of direct-coupled transistor logic circuitry (dctl) as follows: what it is, why it works so well, a method of approach for the design of dctl systems, and how a system works when designed this way.

What It Is

At the top of Fig. 1 is a flip-flop, quite conventional, shown for reference. Below it is a direct-coupled flip-flop; it has no voltage dividers made from resistors, and there is only a single voltage supply. Still, it acts like the conventional flip-flop with one transistor off and one on. The right-hand transistor is on because its base gets nearly all the current from the left resistor. Because it is on, its collector voltage is low, something like 50 mv. This 50 mv is applied to the left base. It is a positive voltage[2] (as are all static voltages in the system) and so is of the opposite polarity to what one would desire to turn off completely, the left transistor. Even so, it is sufficiently near ground, or one might say sufficiently negative, to keep the left transistor effectively off.

The current that flows in a resistor is very nearly constant, regardless of whether the dctl flip-flop is in one state or the other state or changing state. This comes about because of the extremely small range of voltage on a node. In the state shown, the left-hand resistor supplies current to the right base plus some leakage current in the left collector. If the flip-flop were in the other state, the left-hand resistor would furnish collector current for the left stage; the base current of the right transistor, now off, would be negligible.

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[1] R. H. Beter, W. E. Bradley, R. B. Brown, and M. Rubinoff, "Surface-barrier transistor switching circuits," 1955 IRE Convention Record, pt. 4, pp. 139–145.

[2] All voltages would be negative in a system using *p-n-p* transistors.

Why It Works

In order to show why the system works well, several points deserve mention.

1) A transistor can be an excellent (though not perfect) closed switch. Ideally, the right collector in Fig. 1 should go to zero volts, or, even better, to a slight negative voltage in order to shut off the left transistor. Actually, a transistor collector cannot provide zero volts, but it can provide 50 mv or so of positive voltage, which is adequately near zero.
2) When a transistor in a dctl circuit is nominally off, it is actually in the edge of the active region. Its collector current (desirably very low) can be thought of as the collector diode reverse current I_{co} multiplied by a factor involving alpha, the current gain. Transistors are designed to have a high alpha in the active region. This might be expected to result in excessively large collector currents in the nominally off condition. Fortunately, it is generally found that alpha drops to a low value at the low-current edge of the active region. For a typical germanium-alloy transistor, the collector current is reduced by a factor of five to ten because of the reduced alpha at low currents.
3) Nature is favorable in permitting a rapid switch-off. A reverse base current is desirable for fast switch-off.[3,4] With a power supply of only one polarity, it might seem that reverse base current is not possible. However, if the circuit is examined carefully, the emitter diode within the transistor being turned off is found to have voltage across it; this voltage has the proper polarity to drive reverse base current. It may be noted that the reverse base current cannot exceed the value set by the diode voltage (some 200 mv for germanium), and the internal base resistance of the transistor is turned off. Early in the process of switch-off, the voltage on the emitter diode arises from the flow of collector current. Even after this current ceases to flow in the emitter diode, the diode can maintain voltage of the proper sign because of a "memory" of the flow of forward current.
4) Collector leakage current in germanium transistors becomes undesirably high at high temperature, especially with the forward base bias voltage of a dctl system. However, it is found that this

[3] J. J. Ebers and J. L. Moll, "Large-signal behavior of junction transistors," Proc. IRE, vol. 42, pp. 1761–1772; December, 1954.

[4] J. L. Moll, "Large-signal transient response of junction transistors," Proc. IRE, vol. 42, pp. 1773–1784; December, 1954.

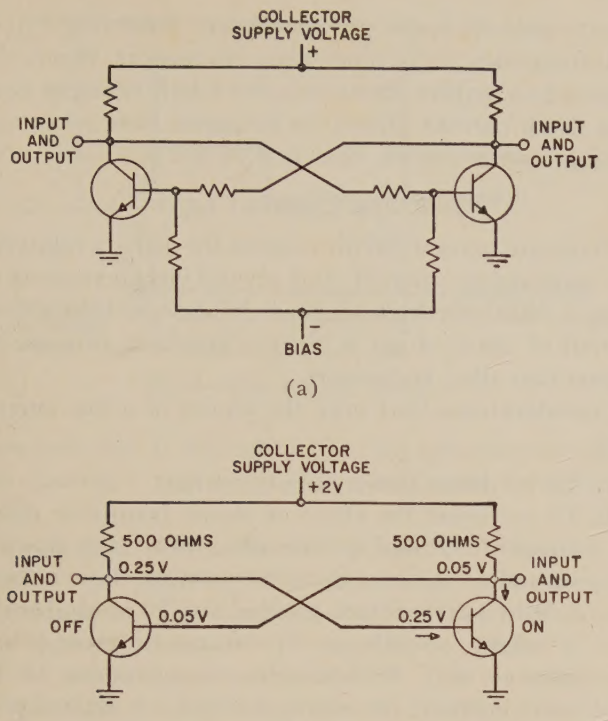

Fig. 1—(a) Simple Eccles-Jordan flip-flop, (b) dctl flip-flop.

effect is less severe in dctl than might be expected. The reason for this is that the forward base bias voltage (which is the collector voltage of an ON transistor) tends to be reduced at high temperature. It appears that the ON collector voltage of germanium-alloy transistors goes down at high temperature because of an increase in alpha.

5) A prime problem of reliability is the fact that some transistors show an increase of collector leakage current with age. In cases where this current has become quite high, it is usually found that the collector current has become strongly dependent on collector voltage. A transistor which has intolerable leakage current at ordinary voltages (*e.g.*, 4.5 volts) is likely to work the same as its well-behaved brothers in a dctl circuit with its inherently low collector voltage. This fact is considered added insurance; the drive toward wholly reliable transistors must not be relaxed.

An Approach to the Design of a DCTL System

A more complete system is shown in Fig. 2. Note the flip-flop, two circuits (one a two-level series circuit) which drive it, and three circuits which might be considered to be driven by it. This system works as follows: suppose the left transistor of the flip-flop is OFF and the right ON. Now, if the single level driver, or both the upper and lower series drivers, become ON, then point X will approach ground, the right transistor of the flip-flop will go OFF, and finally, the left transistor will go ON.

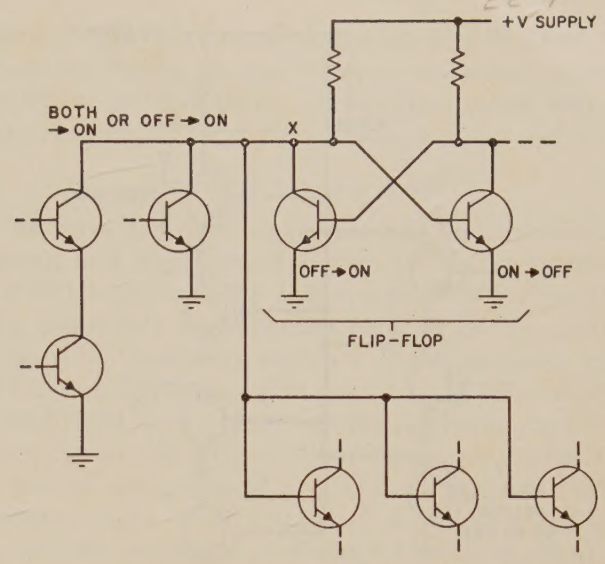

Fig. 2—A typical dctl circuit.

Logical Design Rules and Transistor Requirements

In a configuration like this, the questions arise, "How many transistors can a flip-flop drive?" "How many transistors can be used to drive a flip-flop?" and so on. For convenience the questions will be put in a different form. Note that the transistors in the flip-flop seem to be connected very nearly like the other transistors of the system. In our experience, no good reason has been found for associating a current supply resistor with a flip-flop any more than with the other transistors. It is to be noted that a resistor feeds only collectors and bases. Accordingly, the question to be answered is just this: "How many collectors and bases can be connected to a resistor?" The answer can be thought of as rules for logical design.

To pursue an answer, consider Fig. 3. Here are what may be thought of as successive stages of transistors, which may or may not be a part of a flip-flop. For simplicity, assume that *all* the current-supply resistors are of the same nominal value and depart from this policy only for good reason. (It appears that a single value is practical.)

The currents in Fig. 3 are intended to represent a worst combination of resistor tolerances. The aim is to assure that a transistor will stay OFF when it should be OFF and ON when it should be ON, with a very *worst* pileup of all conditions. This will be referred to as "stability." How can this be assured? Referring to Fig. 3, one can say in general that the current needed by the bases on a node, plus the leakage current of the collectors on that node, must not exceed the current the resistor supplies (in this case 3.5 ma).

Something can be said now about what kind of transistor is desired. It is one with low collector leakage current; one that gives low V_{CE} with a minimum of current feeding an array of bases in parallel and, of course, one

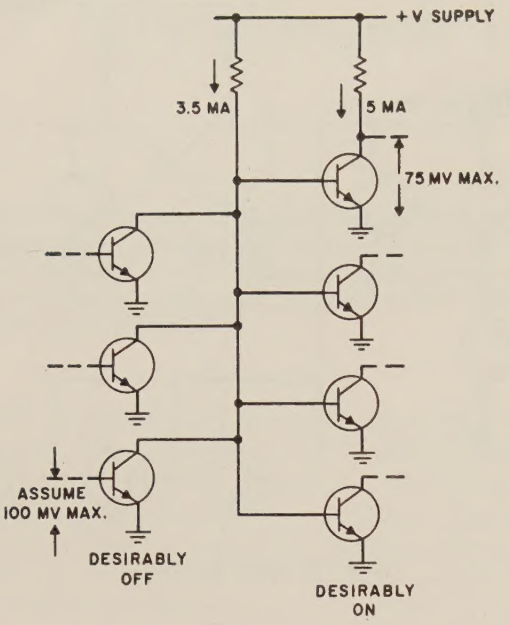

Fig. 3—The problem of static stability.

that is fast enough. Easley[5] describes a set of transistor specifications which, in combination with a proper set of logical design rules, are necessary and sufficient for stability.

An Example of Logical Design Rules

The basic logical design rule we have used for germanium-alloy transistors states merely that the total number of collectors and bases on a node shall not exceed seven. (This applies to all collectors and to bases of transistors in single-level circuits.) Derivation of this rule will now be outlined with the help of Fig. 3. It is the intention that no collector leakage current on the left exceed 0.5 ma at 40°C. (One would like to put a lower value on the current, thus broadening the logical design possibilities, and a higher value on the temperature, but to do either would demand unreasonably tight specifications on the transistor.) To assure the stated low leakage, the forward bias on a left base should never exceed 100 mv. To assure the 100 mv or less in the presence of noise, an ON stage which would drive one of the bases on the left should not exceed a V_C value of 75 mv. Similarly, one should be sure that no collector on the right exceeds 75 mv. The transistor specification is arranged to assure that the latter will be true if the mathematical average per-base drive is 0.5 ma. Thus, the most "allowance" a base or collector will need is 0.5 ma. Therefore, a total of seven bases and collectors can be connected to a node.

If one of the circuits on the right in Fig. 3 were a series circuit, 75 mv (or less) on the top collector would still be needed. With a two-level series circuit, this represents only 37.5 mv per transistor. Assuming typical high-frequency germanium-alloy transistors, this can be expected to require about two and a half times as much base drive current allowance for *every* base on a node driving a series circuit, that is, 1.25 ma per base.

Choice of Current Level

There are several circuit reasons for using a relatively low node-supply current, and several circuit reasons for using a relatively high current. It appears that a node current of about 4 ma is quite a good compromise for germanium-alloy transistors.

Considerations that urge the choice of a low current are:

1) To minimize power-supply current.
2) To minimize the effect of ohmic transistor resistances r_c', r_e', and r_b'. One effect of r_b' is to slow the turnoff of the transistor in question. Low current acts in a rather back-handed way to minimize this r_b' effect, as follows. The transient reverse base current may be somewhat independent of the node current; its maximum value is fixed by r_b'. A low node-current means a low forward base current and low collector current when a transistor is on, which, with a relatively fixed value of transient reverse base current, results in faster turnoff.

Considerations that urge the choice of a high current are:

1) To minimize the effect of capacities on switching time. (Usually a small effect.)
2) To minimize the effect of collector leakage current.
3) To reduce the variation of base currents among bases connected in parallel.[6]
4) To avoid the loss of current gain that occurs in some transistors, particularly certain silicon types, at low current levels.

Crosstalk Problems

In any switching system, it is to be expected that normal operation will produce pulses of current in the ground system. In a high-speed system, fast rising pulses will produce voltage differences in the ground system because of ground inductance. If these voltages interfere with parts of the system, we can say that we have crosstalk, or noise trouble. One of the problems arising from crosstalk is illustrated in Fig. 4. The circuit drawn here is a part of a dctl system, that, for the moment, must stay in the state shown if the system is to work right. It can be thought of as a crosstalk receiver. Imagine that there is a bank of transistors grounded on the left side, driving a bank that is grounded on the right side. These are the crosstalk generators. When these generators switch, a pulse of current appears in the ground conductor and develops a voltage because of ground inductance. This voltage can, of course, be of

[5] J. W. Easley, "Transistor characteristics for direct-coupled transistor logic circuits," this issue p. 60. See (25) and (26); also (23) and (24).

[6] *Ibid.*

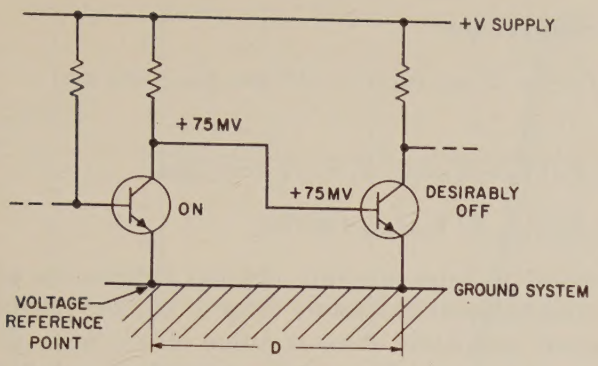

Fig. 4—The crosstalk problem.

either polarity. If the right end of the ground goes negative, the right transistor shown will tend to turn on falsely.

In one experiment, ten surface barrier transistors at the left end drove ten at the right end of a ground plate 14 inches long ($D = 14$ inches) and 5 inches wide. Total current switched was 60 ma and a noise pulse of 40 mv and 0.2 μsec was generated. At 40°C, this is considered to be enough to begin to turn on (falsely) a surface-barrier transistor which has a static base voltage of 75 mv. Germanium-alloy transistors of 7 to 10-mc alpha cutoff frequency were found to generate ground noise about 1/10 the amplitude and ten times the duration of surface-barrier units.

Fortunately, a false signal, even though it propagates, would generally reach a stage that is heavily saturated. Being very brief, the false signal would not turn off the saturated stage, and would propagate no further. However, for best reliability, it seems desirable to make sure that *no* stage switches falsely. To achieve this, our approach has been to minimize ground inductance by mounting transistors very close together.

Where it is necessary to use so many transistors that the ground inductance becomes too large, the total is split into "islands," each of which has tolerably low ground inductance. Since the noise is developed on the ground inductance, and the ground resistance is negligible, the noise amplitude drops off at low frequencies. Accordingly, a low-pass filter can be used in the signal path between islands to attenuate noise. A heavily saturated transistor at the proper place in the signal path has been used for this purpose.

Silicon transistors have the possibility of tolerating a great deal more noise than germanium transistors without false turnon. This is because a silicon transistor requires a great deal of forward base voltage to give excessive collector leakage current—in the neighborhood of 650 mv at room temperature and 350 mv at 75°C.

A second effect of noise must be considered, namely, false turnoff. Where bases are connected in parallel, noise applied between the respective emitters will cause an unbalance of base currents, the bad effect being the reduction of one or more base currents. The effect can be studied in detail by noting that the noise adds to or subtracts from the transistor parameters V_{B1} and V_{B2} defined by Easley.[6] Storage time in transistors reduces this effect, and the effect has not been taken into account directly in the system design to be described.

How One System Works

The rules mentioned were used to build a counter, register, and parity-check system for a core memory, with 800 transistors. In this system, 400 germanium-alloy transistors are mounted on each of two ground plates. The transistors used are Radio Receptor type RR163 (see Appendix). The V_{B1} and V_{B2} specifications of the RR163 have a safety margin (perhaps larger than necessary) to take care of measurement error; the margin will be seen to be 20 mv. These transistors have a minimum alpha cutoff frequency of 7 mc. It is found that signals propagate at about 0.5 μsec per stage, in general agreement with the Ebers-Moll theory.[3,4] The noise in this system is acceptably low.

Perhaps the most interesting aspect of this system is its supply voltage margins. The single supply voltage (nominal 2 volts) can be varied from 0.4 to at least 13 volts. However, changing the single supply voltage does not necessarily show up a weak component because the current ratio (input and output of a stage) tends to remain constant. How can a weak component be found? One can set up, insofar as possible, to feed resistors of alternate stages from a separate supply, and then vary the separate supply; then the current ratio of an individual stage changes so that it becomes heavily saturated or else lightly driven. When this is done, the margins are found to be 1.25 volts to 3.45 volts. It appears that these margins are usually set by transient behavior, by transistors becoming too slow.

The power dissipation of the entire 800 transistors is about 0.25 watt. The power required from the power supply is about 3 watts, most of which is, of course, dissipated in the resistors of the system.

Another piece of equipment built with the same transistors and the same logical design rules was a word generator. In temperature tests of this unit, which uses 119 transistors, operation was satisfactory over a range exceeding −50°C to +65°C. The upper temperature limit was set by the circuits slowing down due to an increase in "hole storage." The fact that the design temperature of 40°C could be exceeded so much is an indication of the size of the safety factor that results from the approach of designing for the most adverse logical design conditions (such as a maximum number of bases on a node) together with a most adverse pileup of component tolerances.

More recently, a complete computer (Leprechaun) has been built[7] using the logical design rules and the form of transistor specification described herein.

[7] J. A. Githens, "The Tradic Leprechaun computer," *Proc. Eastern Joint Computer Conference*, AIEE Special Publication T92, p. 29; December 10–12, 1956.

Conclusion

The object was to evolve design rules for dctl which would assure proper switching and freedom from crosstalk noise trouble under some worst pileup of conditions. By grouping many transistors together on a very small ground plate, and using special circuits between ground plates, crosstalk noise appears tractable. Proper switching can be assured by 1) rules restricting the number of bases and a collectors on a node and 2) the use of transistors which meet a specification evolved for dctl.

Appendix

Electrical Specification—Radio Receptor RR163—July 26, 1955

All values appropriate to measurements at room temperature (25°C).

1) $f_\alpha(V_{CB}=-1.5\text{v}, I_c=-1\text{ ma})\geq 5$ mc
$f_\alpha(V_{CB}=-6, \quad I_c=-1\text{ ma})\geq 7$ mc.

2) $C_c(V_{CB}=-6)\leq 25$ mmf.

3) Storage time[8]

$T_1(I_c=-5\text{ ma}, I_{B1}=-0.5\text{ ma}, I_{B2}=0.5\text{ ma}) \leq 0.5\ \mu\text{sec}.$

4) $|I_c|\,(V_B=V_E=0,\ V_c=-1.5\text{v})\leq 5\mu\text{a}.$

5) $|V_{B1}|_{\min}\geq |V_{B2}|_{\max}+0.02\text{v},$

where the subscripts min and max indicate the minimum acceptable absolute value of V_{B1} and the maximum acceptable absolute value of V_{B2} for a given transistor type. V_{B1} and V_{B2} are defined as follows.

$$V_{B1}=V_{BE}(I_c=-5.0\text{ ma}, I_B=-0.5\text{ ma})$$

$$V_{B2}=V_{BE}(I_c=-5.0\text{ ma}, V_c=-75\text{ mv}).$$

For the RR163, $|V_{B1}|_{\min}=220$ mv, $|V_{B2}|_{\max}=200$ mv.

6) Punch-through voltage, not less than 5 volts.

[8] For definition of T_1, I_{B1}, and I_{B2}, see Moll, *op. cit.*

Transistor Characteristics for Direct-Coupled Transistor Logic Circuits*

JAMES W. EASLEY†

***Summary*—The basic requirement for stability of a direct-coupled transistor logic (dctl) circuit is that a voltage margin exist between the maximum collect-emitter voltage of an "on" unit in the system environment and the minimum base-emitter voltage required for a transistor to be sufficiently "off." This margin has been expressed in terms of the fundamental device parameters: common-base forward and inverse current gain, α_N and α_I; ohmic body resistances of the emitter, collector, and base regions, r_e' and r_c', r_{bIII}; collector saturation current, I_{CO}; and the ratio of the value of α in the vicinity of the "off" state to its value in the vicinity of the "on" state.**

In addition, the connection of bases in parallel results in a dependence of stability on the magnitude of α_I and of r_{bIII} and on the variations of α_N, α_I, r_{bIII}, and I_{CO} among units connected in this manner. Circuit stability requirements have been expressed in terms of these parameters and the effect of their variations is considered.

Methods for the specification of acceptance requirements for dctl transistors and the relation of these specifications to logic design rules are discussed.

* Manuscript received by the PGEC, November 13, 1956; revised manuscript received, January 6, 1958. This work was supported by the Wright Air Dev. Center under Contract AF33-(600)-21536. A summary of this material was presented at the IRE-AIEE-University of Pennsylvania Transistor Circuits Conference, Philadelphia, Pa.; February, 1956.

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I. Introduction

THE design and performance of direct-coupled transistor logic circuits of the type described by Beter, *et al.*,[1] depend to a large extent on the characteristics of the transistors employed. It is reasonable to consider that the circuit elements which are interconnected to form a switching system are the transistors themselves; consequently, the emphasis is shifted from the study of circuit elements such as amplifying stages and bistable circuits to the study of transistor characteristics. It is therefore of interest to relate the circuit variables which are significant in circuit design to transistor parameters, particularly to those which may be related in turn to the physical structure of the transistor through existing design theory.[2]

[1] R. H. Beter, W. E. Bradley, R. B. Brown, and M. Rubinoff, "Surface-barrier transistor switching circuits," 1955 IRE Convention Record, pt. 4, pp. 139–145.

[2] For example, J. M. Early, "Design theory of junction transistors," *Bell Sys. Tech. J.*, vol. 32, pp. 1271–1312; November, 1953.

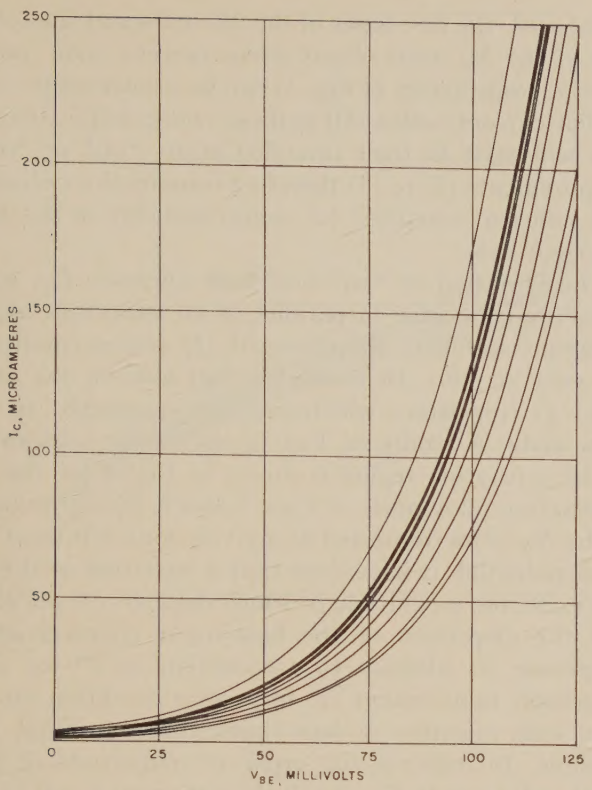

Fig. 1—"Off" state region I_C vs V_{BE}, V_C=0.5 v.

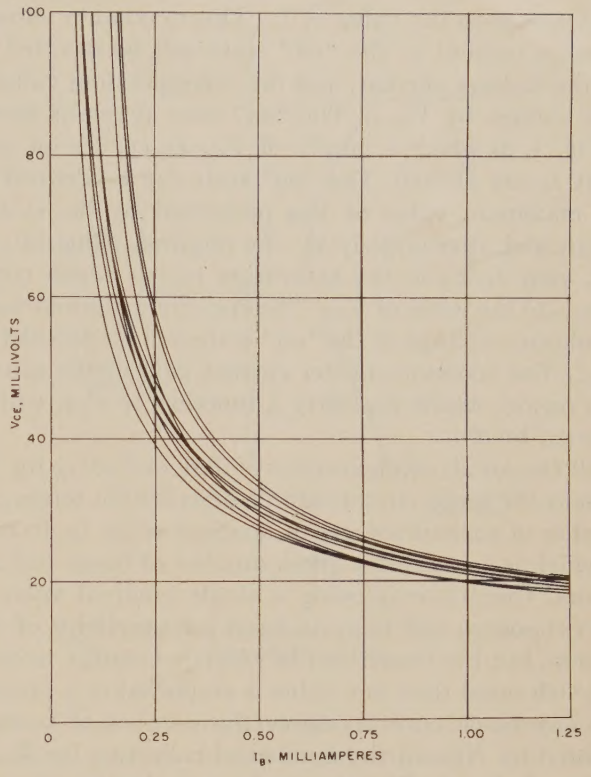

Fig. 2—"On" state region V_{CE} vs I_B, I_C=5.0 ma.

The quantitative material of the paper relates specifically to the dc requirements of parallel circuits, including all those in which the emitters of all transistors are connected to a common ground. This emphasis is based on three factors: 1) In contemporary dctl circuit design the greatest number of transistors in a system is commonly employed in parallel circuits. The Leprechaun Computer of the Tradic Computer Research Program has approximately 90 per cent of its transistors employed in this manner. 2) The circuit design rules for parallel circuits can be specified in a general manner by the stipulation of simple requirements at a single point in the circuit, the current source; whereas for series circuits, requirements must generally be imposed on adjacent sources. The circuit designer has a choice in how these requirements are to be imposed, whereas the choice for parallel circuits is largely determined by the transistor itself. 3) The qualitative nature of the requirements imposed on the transistor is essentially the same for both series and parallel circuits. The requirements for any given form of series circuit connection can be qualitatively determined by the same method, applied specifically to parallel circuits in this paper.

The expression of sufficient conditions for the circuit stability of parallel circuits in the most stringent case and a qualitative consideration of the relevant transistor characteristics will be considered in Section II. Section III is concerned with the expression of these circuit conditions in terms of fundamental device parameters and the effect of the individual parameters on circuit capabilities. A qualitative discussion of addition factors encountered in series circuits follows in Section IV. Some methods for specifications of acceptance limits are presented in the Appendix.

II. Stability Requirements

The basic requirement for the dc stability of dctl circuits is the existence of an adequate voltage margin Δ between the maximum collector-emitter voltage V_{CE} of an "on" unit in the system environment and the minimum base-emitter voltage V_{BE}, required for a transistor to be sufficiently "off." This margin must be equal to or greater than the maximum spurious signal, pickup or crosstalk, which tends to turn an "off" unit "on." In order to discuss the relation between "on" and "off" units, as employed in the system, and the requirements thereby imposed on both logic design and transistor characteristics, it is helpful to have some general definition of these states and a terminology to describe them.

The transistor in the "on" state is in the saturation region near the boundary between the active and saturation regions. The transistor in the "off" state is in the active region near the boundary between the active and cutoff regions. These two regions of operation are shown in Figs. 1 and 2 for a group of ten germanium-alloy transistors of a type exhibiting satisfactory characteristics for dctl application. The "off" state region is shown in Fig. 1, in which a family of I_C-V_{BE} curves for constant V_C are plotted. The "off" state can be defined by the specification of a maximum value of collector current I_C, permitted by the system design or alternatively by the maximum allowed value of V_{BE} which

corresponds to the value of I_C. This maximum allowed collector current in the "off" state will be denoted by I_L, the leakage current, and the corresponding value of base voltage by $V_{B\,\text{off}}$. The "on" state region is shown in Fig. 2, in which a family of V_{CE}-I_B curves for constant I_C are plotted. The "on" state can be defined by the maximum value of V_{CE} permitted by the system design and alternatively by the required value of current gain I_C/I_B in the saturation region which corresponds to the value of V_{CE}. The maximum allowed value of collector voltage in the "on" state will be denoted by $V_{C\,\text{on}}$. The common-emitter current gain in the saturation region, which is clearly a function of V_{CE}, will be denoted by β^*.

All the circuit configurations of dctl, excluding for the present the series circuit, can be described in terms of a number of current sources of nominal value I_S, to each of which is connected a given number of bases and collectors. Circuits employing a single nominal value of current source will be considered for simplicity of discussion, but the results can be extended readily to cases in which more than one value is employed in a system. For any given current source the number of bases is denoted by N_B and the number of collectors by N_C, as shown in Fig. 3. The circuit design rules can then be expressed simply by a set of allowed pairs of maximum N_C, N_B values. There is no loss of generality if it is considered that the N_C collectors are those of "off" units and the N_B bases are those of "on" units. The most stringent case then requires the satisfaction of the conditions that

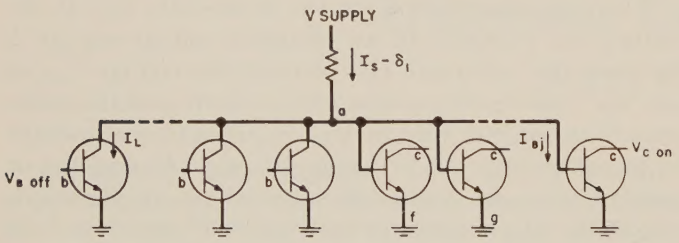

Fig. 3—Parallel circuit schematic—general nodal representation.

$$N_C I_L(V_{B\,\text{off}}) + \sum_{j=1}^{N_B} I_{Bj} \leq I_S - \delta \qquad (1)$$

and

$$I_{Bj}\beta_j^*(V_{C\,\text{on}}) \geq I_S + \delta_2 \qquad (2)$$

where I_S is the nominal value of the supply current and δ_1 and δ_2 are its maximum negative and positive variations. These supply current variations are due to variations from nominal of supply resistor values and to the difference in value of voltage at the current node (point a of Fig. 3). This depends on whether the bases connected to that node are of "off" or "on" transistors. If, in addition to requirements (1) and (2), the requirement

$$V_{B\,\text{off}} \geq V_{C\,\text{on}} + \Delta \qquad (3)$$

is imposed, the free bases of the N_C units and the collectors of the N_B units of any given current node (points b and c, respectively of Fig. 3) can be connected to other similar current nodes. All units so connected in the system will exist in their intended state, "on" or "off."[3] Requirements (1) to (3) therefore constitute a necessary and sufficient condition for circuit stability in the most stringent case.

The variation of "on" unit base currents I_{Bj}, when bases are connected in parallel, is an important aspect of circuit stability. Requirement (2) places conditions not only on the jth transistor, but also on the other (N_B-1) transistors which are base-connected to the same node. A family of V_{BE}-I_B curves for constant I_C in the saturation region is shown in Fig. 4 for the ten germanium-alloy units of Figs. 1 and 2. Since the bases of the N_B units connected at a given node will be at the same potential, it is evident that a variation of the I_{Bj} will exist, the magnitude of which depends on the slope and the dispersion of the base-input characteristics. Therefore, in addition to a condition on β^* for each transistor, requirement (2) imposes a condition on the form and variation of base-input characteristics. For example, to indicate the order of magnitude of this effect, reference to Fig. 2 will show that an $I_B=0.25$ ma for which $I_C/I_B=20$ results in a $V_{CE}\leq 60$ mv, which is a sufficiently low value of collector-emitter voltage for an "on" unit. In this region of saturation Fig. 4 indicates that, on the average, a maximum variation among base-connected units of I_{Bj} equal to 0.2 ma can be expected; if sufficient voltage (indicated by line a-a of Fig. 4) is applied to supply 0.25 ma to the base drawing the lowest current, the base drawing the highest current will require approximately 0.45 ma. Therefore, for this transistor type, base currents of "on" units connected to a given node may vary approximately by a factor of two.

The spread in the distribution of base currents among units base-connected at a given node may be increased from the spread which results from the variation of transistor characteristics alone. This is a result of the possible introduction of a spurious voltage signal in any of the paths between the current node and the connections of all emitters of these N_B units to the common

[3] It should be noted that the value of Δ in the limiting case, given by

$$\Delta = V_{B\,\text{off}} - V_{C\,\text{on}},$$

is the quantity which describes the margin of stability and not the voltage swing of the collector between the "on" and "off" states given by

$$\delta V_C = V_{C\,\text{off}} - V_{C\,\text{on}}.$$

If one considers either nominal or minimal values,

$$V_{C\,\text{off}} = V_{B\,\text{on}}$$

and consequently (5) may be written as

$$\delta V_C = V_{B\,\text{on}} - V_{C\,\text{on}}.$$

Therefore, since it is clear that $V_{B\,\text{on}} > V_{B\,\text{off}}$, $\delta V_C > \Delta$, and the existence of a given minimum δV_C is not a sufficient condition in itself, some minimum Δ exist.

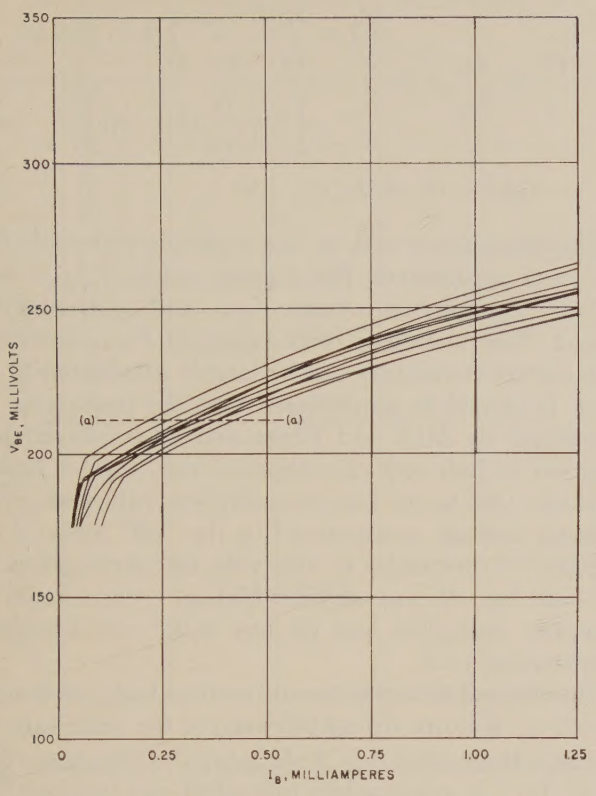

Fig. 4—"On" state region V_{BE} vs I_B, I_C=5.0 ma.

ground, such as in the path *a-f-g-a* of Fig. 3. If this spurious signal is of a polarity which increases the unbalance of base currents and has sufficient magnitude, one or more units, nominally "on," will turn "off." This effect is equivalent to a vertical translation of a V_{BE}-I_B curve of Fig. 4. The base-emitter voltage margin, required to include this effect which is incorporated into both transistor specification and circuit design, will be denoted by Δ'.

In the following discussion of a parametric description of transistor characteristics, required to satisfy the above conditions, it has been convenient to divide the problem arbitrarily into two parts. Consideration is given 1) to the dependence of Δ, corresponding to a given value of applied I_B/I_C and allowed leakage current I_L on transistor parameters, and 2) to the factors involved in the distribution of base currents among "on" units connected to a given node. This is a matter of convenience only, and the two aspects are not independent when the complete performance of a transistor type for dctl application is considered. A manner of empirical evaluation of a transistor type which permits a semi-quantitative separation of these aspects will be outlined in the Appendix.

III. Parametric Expression of Stability Requirements

A means of expressing the dc stability requirements of the preceding section in terms of transistor parameters is provided by the generalized two-terminal-pair theory of junction transistors developed by Ebers and

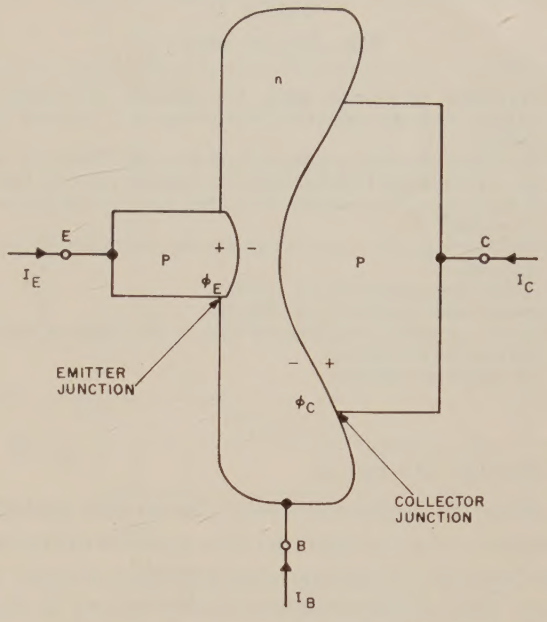

Fig. 5—Junction transistor—generalized geometry (Ebers-Moll theory).

Moll.[4] These authors have given, for the generalized-geometry junction transistor shown in Fig. 5, a pair of current-voltage relations

$$I_E = -\frac{I_{EO}}{1-\alpha_N\alpha_I}\left(e^{q\Phi_E/kT}-1\right) + \frac{\alpha_I I_{CO}}{1-\alpha_N\alpha_I}\left(e^{q\Phi_C/kT}-1\right) \quad (4)$$

$$I_C = +\frac{\alpha_N I_{EO}}{1-\alpha_N\alpha_I}\left(e^{q\Phi_E/kT}-1\right) - \frac{I_{CO}}{1-\alpha_N\alpha_I}\left(e^{q\Phi_C/kT}-1\right) \quad (5)$$

and the equality

$$\alpha_I I_{CO} = \alpha_N I_{EO}. \quad (6)$$

The quantities Φ_E and Φ_C are the junction voltages, for which the positive sense is a voltage drop from p to n material. The other quantities are listed in Table I. In deriving these equations Ebers and Moll assumed that the minority carrier density is sufficiently small, the carrier flow is governed by the linear diffusion equation, and there are no drift fields in the base layer except at the junctions. Unpublished calculations by Moll indicate that the relations have equivalent validity even in the presence of "built-in" drift fields, as would be encountered in a diffused-base transistor.[5,6]

[4] J. J. Ebers and J. L. Moll, "Large-signal behavior of junction transistors," Proc. IRE, vol. 42, pp. 1761–1772; December, 1954.

[5] C. A. Lee, "A high frequency diffused base germanium transistor," *Bell Sys. Tech. J.*, vol. 35, pp. 22–23; January, 1956.

[6] M. Tanenbaum and D. E. Thomas, "Diffused emitter and base silicon transistors," *Bell Sys. Tech. J.*, vol. 35, pp. 1–34; January, 1956.

TABLE I
BASIC DEVICE SYMBOLS

α_N = Transistor dc current gain with emitter functioning as an emitter, and the collector functioning as a collector (normal alpha).
α_I = Transistor dc current gain with emitter functioning as a collector and collector functioning as an emitter (inverse alpha).
I_{EO} = Volume saturation current of emitter junction with zero collector current.
I_{CO} = Volume saturation current of collector junction with zero emitter current.
r_e' = Ohmic body resistance of emitter.
r_c' = Ohmic body resistance of collector.
r_{bIII} = Ohmic spreading resistance of base in the region of saturation.
k = Boltzmann's constant.
T = Temperature °Kelvin.

The Stability Margin, Δ

In order to apply these relations to dctl stability requirements, it is necessary to take account of the current dependence of the normal and inverted α's and consequently their different values in the regions of the "on" and the "off" states. This has been expressed in the ratio of the current gain at current levels of the order I_L to that at current levels of the order of I_S and is denoted by κ,

$$\kappa = \frac{\alpha(I_L)}{\alpha(I_S)}. \tag{7}$$

From (6) the same value of κ applies to both the normal and inverted α of any given transistor, and for the level of supply currents likely to be employed in dctl circuitry, $\kappa \leq 1$. In the expressions that follow, the voltages and currents have been written in terms of their absolute values.

For a given value of leakage current I_L, $V_{B\,\text{off}}$ is given to good approximation by

$$V_{B\,\text{off}} = \frac{kT}{q} \ln \frac{(1 - \kappa^2\alpha_N\alpha_I)}{\kappa\alpha_I} \frac{I_L}{I_{CO}} \tag{8}$$

for all values of I_L such that

$$I_L \gg \left(\frac{I_{CO} - \alpha_N I_{CO}}{1 - \alpha_N\alpha_I}\right)$$

which, in general, will be satisfied.

For a given collector and base current, $V_{C\,\text{on}}$ is given by

$$V_{C\,\text{on}} = \frac{kT}{q} \ln \frac{1 + \frac{I_C}{I_B}(1 - \alpha_I)}{\alpha_I\left[1 - \frac{I_C(1 - \alpha_N)}{I_B\alpha_N}\right]} + I_C r_c' + (I_C + I_B) r_e'. \tag{9}$$

The value of Δ, corresponding to a given allowed value of leakage current I_L and values of collector and base current in the "on" state of I_C and I_B, respectively, is therefore given by

$$\Delta = \frac{kT}{q} \ln \frac{I_L}{I_{CO}} + \ln \frac{\left(1 - \frac{I_C}{I_B}\frac{1 - \alpha_N}{\alpha_N}\right)(1 - \kappa^2\alpha_N\alpha_I)}{\kappa\left[1 + \frac{I_C}{I_B}(1 - \alpha_I)\right]} - I_C r_c' - (I_C + I_B) r_e'. \tag{10}$$

The dependence of Δ on I_{CO} is readily separable from the other parameters. For a given value of I_L, a small value of I_{CO} permits a large $V_{B\,\text{off}}$ and consequently a large Δ. The inherently large values of $V_{B\,\text{off}}$ associated with silicon transistors can be largely attributed to this term. It should be emphasized that the parameter I_{CO}, as defined by Moll and Ebers and as employed here, does not include any contribution from surface leakage currents. Due to the exceptionally low values of reverse collector-voltage encountered in the "off" state of dctl circuitry of the order of 0.2 volt for germanium and 0.7 volt for silicon, surface leakage components are generally negligible and do not make any significant contribution to I_L.

The effect of the collector and emitter body resistances, r_c' and r_e', is quite straightforward in the reduction of Δ by the voltage drop $I_C r_c' + (I_C + I_B) r_e'$. If the magnitude of $(r_c' + r_e')$ is appreciable, this effect can frequently be reduced to a sufficiently low value by operating the circuit at a low current level. For germanium-alloy and certain other types, these terms are negligible. The resistance r_e' has an additional effect in that the collector-emitter voltage for constant I_C is not a monotonically decreasing function of I_B but passes through a minimum. If this effect is pronounced, a reduction in Δ may occur in cases wherein the maximum allowed number of bases N_B is not connected or wherein the maximum total leakage current $N_C I_L$ is not drawn at a given node so that "on" units are driven considerably farther into saturation than the limit set by the "most stringent case." This effect is illustrated in Fig. 6 in which curve *A* has been obtained from a germanium-alloy transistor for which $r_e' \simeq 0$, and curve *B* has been obtained from the same transistor with 5 ohms artificially inserted in series with the emitter. In the following discussion of the effects of α_N, α_I, and κ, the effects of the body resistances will be absorbed for convenience in the change of variable

$$V_{CE'} = V_{CE} - [I_C r_c' + (I_C + I_B) r_e']. \tag{11}$$

The dependence of Δ on α_N and α_I is more complex than the preceding, as the values of these parameters affect both the "on" and "off" state characteristics. The effect of α_N and α_I will first be separated in a first-order or limiting case consideration of the "on" state characteristics. This will be followed by consideration of the combined effect on the "on" state and, in conjunction with κ, on the "off" state and consequently on Δ.

The normal alpha sets the upper limit on the obtainable fanout at a given current node, as denoted in (1) by N_B. This is shown schematically in Fig. 7 in which

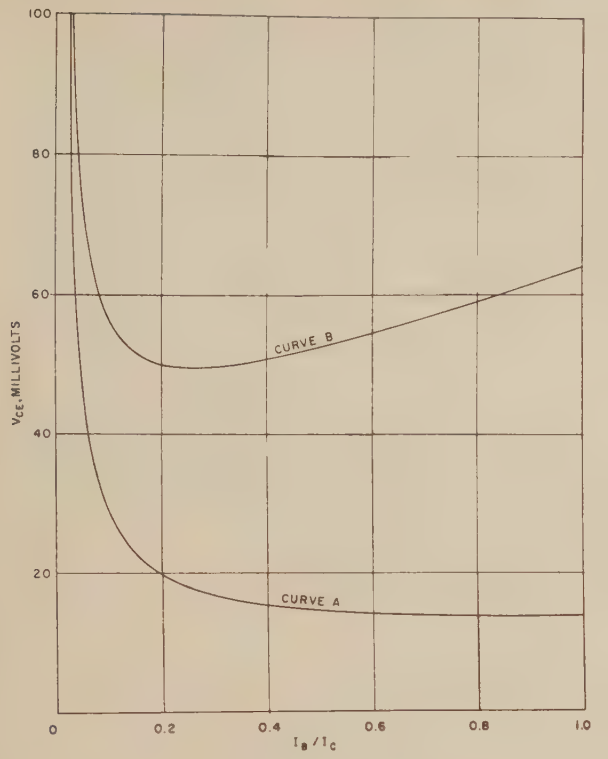

Fig. 6—Effect of r_e' on collector-emitter saturation characteristic.

the significant characteristics of the "on" state region are indicated in a diagram of V_{CE}' vs I_B/I_C. A sufficiently good approximation is to consider this curve as approaching a vertical asymptote, $I_B/I_C=(1-\alpha_N)/\alpha_N$, for small values of I_B/I_C and thereby setting an absolute lower limit for the I_{Bj} of (1) and (2). Eq. (2) will require values of I_{Bj} substantially larger than this lower limit which corresponds to points along the knee of the V_{CE}'-I_B/I_C curve. However, since the vertical asymptote, and consequently the knee of the curve, is translated towards the V_{CE}' axis by increasing α_N, a large value of α_N results in a small $V_{C\ on}$ for any given I_B/I_C, other parameters α_I, r_e', and r_c' being equal.

The first-order effect of the inverse alpha can be expressed in terms of the horizontal asymptote $V_{CE}'=kT/q \ln 1/\alpha_I$ which is approached by V_{CE}' for values of $I_B/I_C \gg (1-\alpha_I)$. The value of α_I therefore sets the lower limit on $V_{C\ on}$ for any value of I_B/I_C. The normal region of "on" operation in dctl circuitry is in the knee of the V_{CE}-I_B/I_C curve, and similar to the consideration for α_N, a large value of α_I results in a small $V_{C\ on}$ for any given I_B/I_C, other parameters being equal.

The combined effect of α_N and α_I on the "on" state characteristics can be expressed in terms of $\beta^*(V_{CE})=I_C/I_B$, the current gain in the saturation region. The quantity β^* is given from (9) by

$$\beta^* = \frac{\alpha_I - e^{-qV_{CE}/kT}}{(1-\alpha_I)e^{-qV_{CE}/kT} + \dfrac{\alpha_I}{\alpha_N}(1-\alpha_N)}. \qquad (12)$$

In Fig. 8, β^* is plotted as a function of V_{CE} for a number of values of α_N and α_I. A compromise between β^* (and

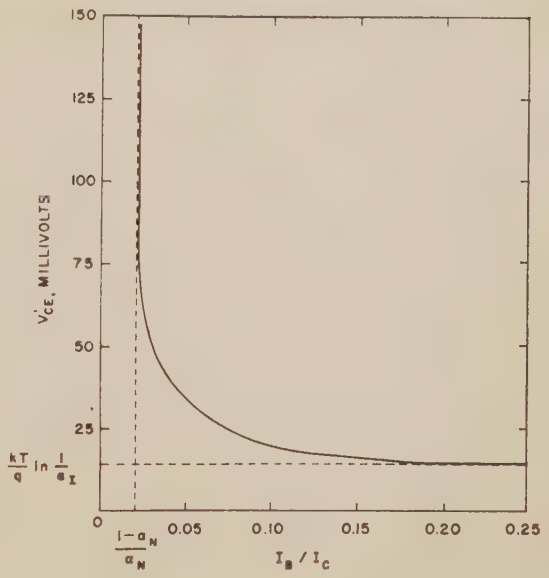

Fig. 7—Asymptotic behavior, collector-emitter saturation characteristic.

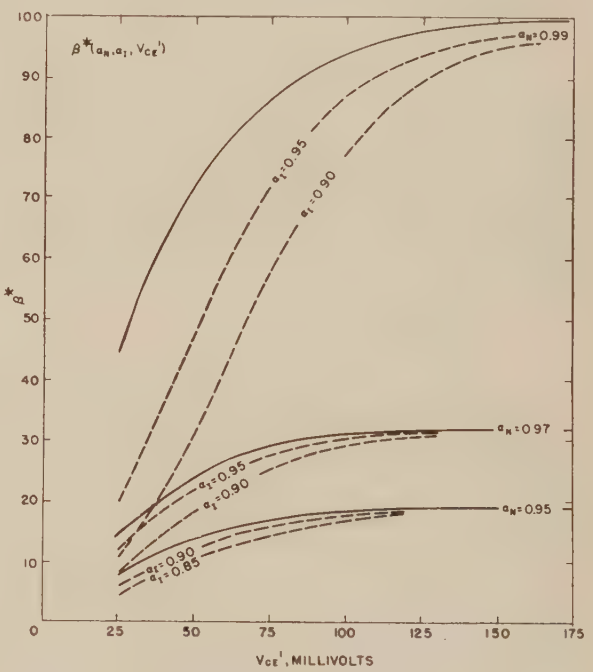

Fig. 8—Common-emitter gain in saturation region, β^*. Solid lines pertain to the symmetric case, $\alpha_I=\alpha_N$.

therefore obtainable N_B) and $V_{C\ on}$ (and therefore obtainable Δ) is one of the many encountered in adjusting circuit design rules to a given transistor.

In addition to their effect on the "on" state quantity $V_{C\ on}$, the parameters α_N and α_I affect the "off" state quantity $V_{B\ off}$. This comes about predominantly through the term $(1-\kappa^2\alpha_N\alpha_I)$ of (8) and (10). In order to obtain a large $V_{B\ off}$ for a given allowed I_L, the coefficient of I_L in the argument of the ln of (8) should be as small as possible. Both α_N and α_I are advantageously large for the optimum characteristics of the "on" state. Therefore, a low value of κ, or a marked current dependence of the α's, in the vicinity of I_L provides the

remaining means of obtaining a large $V_{B\ off}$. In general, of course, the transistors found suitable for dctl have obtained an adequately high $V_{B\ off}(I_L)$ and low $V_{C\ on}(I_B/I_C)$ and consequently a sufficiently large Δ by some compromise among the effects of these parameters. An idea of the regions of parameter values, for which the combined effect of any set of values for α_N, α_I, and κ is to increase or decrease Δ from that obtained with any other set of parameter values, can be obtained from Fig. 9 in which the regions in the α_N-κ plane, for which $\delta\Delta/\delta\alpha_I$ is greater or less than zero, are shown for a given value of applied $I_C I_B$. This conflict is primarily of interest for germanium transistors since present-day silicon switching transistors κ, and to a lesser degree α_N, are sufficiently low so that $(\delta\Delta/\delta\alpha_I) > 0$. It is this current dependence of α, in addition to the low value of I_{CO}, which leads to the high values of $V_{B\ off}$ observed in these silicon transistors. These units are frequently unsymmetric, hence, the adverse effect of α_I on the "on" state characteristics. However, the $V_{B\ off}$ is sufficiently large that values of Δ many times those which can be obtained with germanium can be realized for equivalent I_L and I_C/I_B, within the limits of the upper bound of I_C/I_B set by α_N. It is of interest to note that the parameter κ, which is important in the dctl application of a transistor, owes its existence in part to the effect of surface-recombination.[7] The effect of this parameter is particularly important in a high-alpha, symmetric transistor, such as encountered among germanium-alloy types.

The Variation of Base Currents

The variation of the base currents I_{Bj} of (1), among the N_B transistors connected to a given current node in the absence of any spurious signal, depends on the slope and dispersion of the base-input characteristics. This effect is illustrated schematically in Fig. 10 in which the envelope of a family of V_{BE}-I_B curves is indicated by the bounding curves labeled (*a*) and (*b*). The points along the V_{BE}-I_B curves of this schematic family, at which the collector voltage of any given transistor is less than some defined $V_{C\ on}$, are indicated by the various X. In order for all transistors whose bases are connected to a given node to be "on," the voltage at the node must be equal to or greater than the highest base voltage required by any one of the N_B transistors in the "on" state. This voltage is indicated by V_B' in the diagram. At this voltage the limiting transistor which corresponds to envelope (*a*) draws a base current equal to I_B' and all other transistors draw base currents, $I_B' \leq I_{Bj} \leq I_B''$. Since it is not practical to determine the V_{BE}-I_B characteristic of every transistor employed in a system, it appears reasonable for circuit design purposes to consider the maximum current, needed to be drawn, as equal to

[7] V. M. Webster, "On the variation of junction-transistor current-amplification factor with emitter current," PROC. IRE, vol. 42, pp. 914–920; June, 1954.

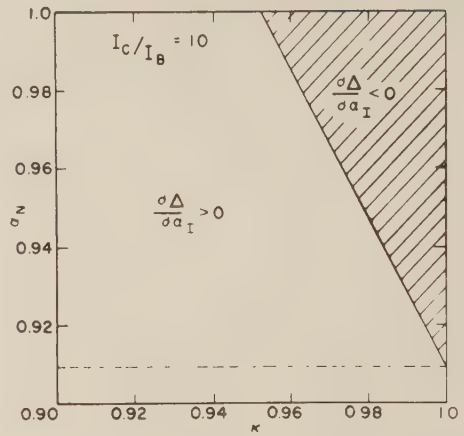

Fig. 9—Regions in which Δ is an increasing or decreasing function of α_I. Values of α_N below the dashed line are insufficient for saturation with $I_C/I_B = 10$.

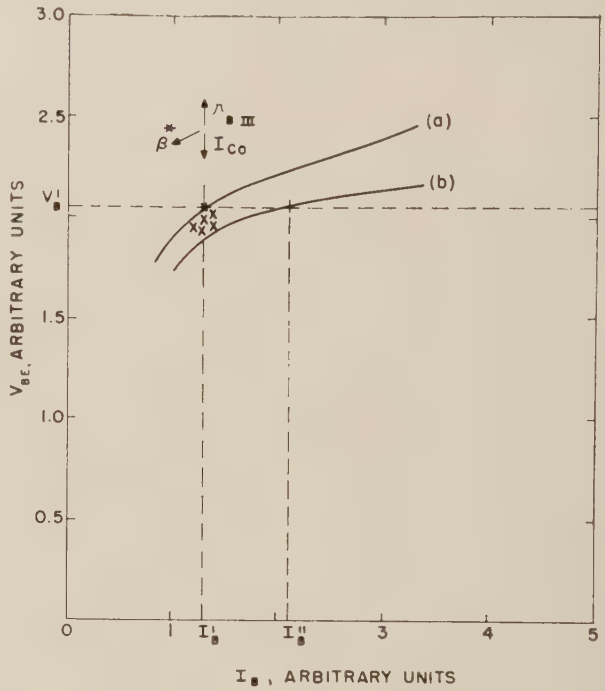

Fig. 10—Distribution of "on" state base currents—schematic.

$$I_{Breq} = I_B' + (N_B - 1)I_B'' \geq \sum_{j=1}^{N_B} I_{Bj}. \qquad (13)$$

The base-input characteristics which are advantageous for the dctl application of a transistor are those possessing a large slope and a small dispersion, as can be seen from a consideration of Fig. 10. The base-emitter voltage in the saturation region is given by

$$V_{BE} = I_B r_{bIII} + \Phi_E + (I_C + I_B) r_e' \qquad (14)$$

where r_{bIII} is the ohmic base resistance in the saturation region. The quantity r_{bIII} is always less than or equal to the active region ohmic-base spreading resistance as defined by Early[2] and may be reduced in some cases, such as for grown-junction transistors, by almost two orders of magnitude. It is convenient to absorb the term $(I_C + I_B) r_e'$ by the change of variable

$$V_{BE}' = V_{BE} - (I_C + I_B)r_e'. \tag{15}$$

The relations of Ebers and Moll[4] yield for the saturation region

$$V_{BE}' = I_B r_{bIII} + \frac{kT}{q} \ln \left[\frac{I_B + (1 - \alpha_I)I_C}{I_{EO}} \right], \tag{16}$$

so that the slope of the V_{BE}'-I_B characteristic is given by

$$\frac{\partial V_{BE}'}{\partial I_B} = r_{bIII} + \frac{kT}{qI_C} [I_B/I_C + (1 - \alpha_I)]. \tag{17}$$

The contribution from the emitter junction potential for any given ratio of applied currents I_B/I_C, and therefore the region of saturation in which the "on" state is defined, varies inversely then with the collector current and depends on the magnitude of the inverse alpha.

The efficacy of a large r_{bIII} is evident from (17) but, as will be discussed, the variations of r_{bIII} as well as other parameters should be advantageously small. An upper limit on the value of r_{bIII} is imposed by the transient response of an "off-going" unit. The reverse base current during the transition of a transistor from the "on" to the "off" state is given by

$$I_{B2}(t) = \frac{\Phi_E{}^{(2)}(t) - V_{CE}{}^{(1)}(t)}{r_{bIII}(t)} \tag{18}$$

where $\Phi_E{}^{(2)}$ is the emitter-junction potential of the "off-going" unit and $V_{CE}{}^{(1)}$ is the collector-emitter voltage of the preceding "on-going" unit. These quantities and r_{bIII} are all functions of time during the transition. Therefore, as the reverse current I_{B2} is inversely proportional to r_{bIII}, the storage and turnoff times of the "off-going" unit can be expected to increase with increasing r_{bIII}.[8]

The dispersion of input characteristics among transistors is due to variations in I_{EO}, α_I, and r_{bIII}. In addition, variations in α_N will contribute to dispersion of the "on" points, as indicated by the X in Fig. 10. The qualitative relation of this dispersion to the variation of parameters is illustrated by arrows in Fig. 10 which indicate the direction of movement of an "on" point which corresponds to a positive change in r_{bIII}, I_{EO}, and β^*. In order to maximize the yield of transistors satisfactory to dctl, it is then necessary to minimize the variations of these parameters.

IV. Series Circuit Considerations

The dc stability requirements of series circuits cannot be expressed as simply as those of parallel circuits and a greater choice in circuit design is available for their satisfaction. The two-element series circuit, shown in Fig. 11, will serve as an example for a qualitative discussion of the principal considerations.

[8] J. L. Moll, "Large-signal transient response of junction transistors," Proc. IRE, vol. 43, pp. 1773–1784; December, 1954.

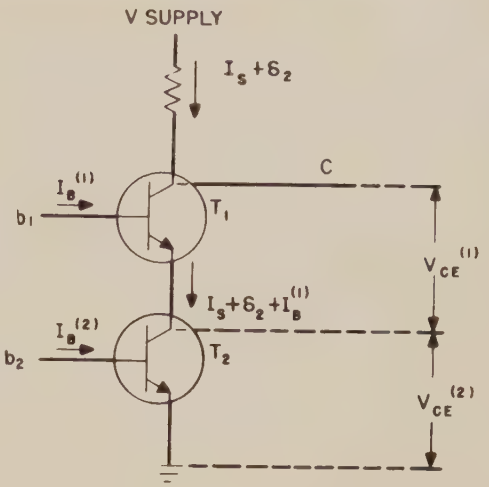

Fig. 11—Series circuit schematic—(2 element).

One additional requirement, if the point c of Fig. 11 is to connect to other current nodes and satisfy the same requirements as those of Section III, is that the "on" state collector-emitter voltages of T_1 and T_2 must satisfy the condition

$$V_C{}^{(1)}{}_{on} + V_C{}^{(2)}{}_{on} \leq V_{C\,on} \tag{19}$$

where $V_{C\,on}$ has the same value as in (4). Another is brought about by the increase of the maximum collector current of T_2 by the addition of the base current of T_1, so that the β^* requirements for the two transistors are now

$$I_B{}^{(1)}\beta^{*(1)} \geq I_S + \delta_2 \tag{20}$$

and

$$I_B{}^{(2)}\beta^{*(2)} \geq I_S + \delta_2 + I_B{}^{(1)}. \tag{21}$$

A third additional factor is realized when the voltage between the base of T_1 and ground is increased above that of an equivalent operating point for parallel circuits by the value of $V_{CE}{}^{(2)}$ of T_2; this increase effects the distribution of base current at a given node.

The effect of these additional factors is to place the emphasis on the β^* of the transistor, thus making the problem of the distribution of base currents primarily a circuit problem rather than a transistor one. For a given transistor, requirements (19) to (21) can be satisfied generally by decreasing the ratio I_C/I_B corresponding to the "on" state so that the required lower values of V_{CE} are obtained and by a circuit design which sets a minimum value on $I_B{}^{(1)}$ and $I_B{}^{(2)}$ and a maximum value on $I_B{}^{(1)}$. The latter can assume the form of restrictions imposed on the nodes to which bases (b_1) and (b_2) are attached, or possibly the insertion of a resistive element in series with the base of either or both transistors.

V. Conclusion

The circuit requirements for the dc stability of dctl parallel circuits have been expressed in a general form. Through application of the dc theory of junction transis-

tors of Ebers and Moll and consideration of the alpha current dependence, these circuit requirements can be expressed in terms of fundamental device parameters. Therefore, a connection can be effected between circuit design capabilities and transistor structure for dctl circuitry.

This type of circuitry places a strong emphasis on the reduction of parameter variations, particularly of α_I, r_{bIII}, and I_{EO}, and to a somewhat lesser degree of α_N, in order to minimize the spread of base-input characteristics and base current thresholds for the "on" state. The adverse effect of this spread on circuit capabilities is reduced by an increase in average r_{bIII} and α_I. In addition, the optimum dctl transistor exhibits a high value of α_N, a low value of I_{CO}, and is symmetric or near symmetric. The ohmic body resistances, r_c' and r_e', should be as small as possible. This is particularly the case for the emitter body resistance r_e'. The current gain should fall off advantageously at current levels corresponding to the collector current in the "off" state. This generalization should be regarded as a guide to aspects which may cause a transistor to be unsatisfactory for dctl application since one or more of these characteristics will in general be lacking to some degree in satisfactory transistors. For the evaluation of any given transistor, reference should be made to Section III.

Although the analysis has been based on the requirements of parallel circuits, the same methods may be applied to the less general problem of series-circuit design.

VI. Appendix

Specification of Acceptance Requirements

Since the circuit variables of interest in dctl circuitry are not related simply to fundamental device parameters, it is not possible to stipulate an efficient acceptance limit specification in terms of these parameters and their variations which, at the same time, constitutes a sufficient condition for circuit stability. Efficiency in this sense refers to a specification which, by its form, rejects the minimum number of units which would provide adequate circuit operation. In this section, specifications are developed which are related to the performance of the transistor as a simple switch and which determine the combined effects of the various interacting parameters and their variations. The specifications of acceptance limits are based on the assumed requirement of complete interchangeability of transistors in a system or in some subelement of a system employing a single type of transistor. The type of circuit specifically considered is one employing a single nominal value of supply current and resistor, but the form of the specification can be adapted to a less uniform system and the general mode of specification will be unchanged. These specifications and associated circuit design rules represent a sufficient condition for only parallel circuits.

"Off" State Specification

The specification of acceptance limits for the "off" state can be accomplished by stipulating the maximum allowed collector current, corresponding to the maximum value of base-emitter voltage $V_{B\,off}$, as

$$I_C(V_{CE} \tilde{>} V_{B\,on},\ V_{BE} = V_{B\,off}) \leq I_L' \qquad (22)$$

where for practical purposes V_{CE} can be any small voltage satisfying the above requirement. A larger value of voltage merely increases the contribution of surface leakage current and is not appropriate to this application except as a possible indication of surface conditions in a particular transistor, nonrepresentative of its type. This specification sets upper limits on the multiplied I_{CO} of (8) and therefore depends on the combined effect of I_{CO}, α_N, α_I, and κ. The limit value of current has been denoted by I_L' rather than the unprimed I_L of preceding sections to indicate that I_L is generally the current at some elevated temperature, whereas the specification may be written for a room temperature measurement. If this is the case, I_L' denotes a reduced value at room temperature such that the current under the same voltage conditions does not exceed the value I_L at some elevated temperature of circuit operation. If a separate determination of the temperature dependence of $I_C(V_{BE})$ for any given transistor type is to be avoided, or in cases such that $I_C(V_{BE})$ at room temperature is sufficiently small as to constitute a difficult quantity on which to base a temperature extrapolation, then a specification at the design-maximum temperature of operation is preferable. The latter is generally the case for a silicon transistor.

"On" State Specification

A specification for the "on" state must impose two general types of restrictions. It must impose some restriction on β^* and on the slope and dispersion of the base-input characteristics. The specification may be of a form in which these two aspects are considered as a whole or one and in which an explicit separation is made. Two types of specifications will be outlined. The first is of the former type and is applicable to transistors possessing an r_{bIII} sufficiently large to permit effective use in the basic form of the circuit as shown in Fig. 3. The second is of the latter type and is applicable to transistors with values of r_{bIII} sufficiently small so that it is difficult to achieve a reasonably small spread of base currents among "on" units connected at a given node. With these transistors an external base resistor may be employed to equalize the base currents.

The "on" state characteristics are of course temperature dependent but, contrary to the "off" state degradation of Δ at elevated temperature, the value of V_{CE} for a given I_C/I_B generally decreases with increasing temperature, thereby tending to increase Δ. This is due to the increase of both α_N and α_I with increasing temperature. The magnitude of the effect, however, is con-

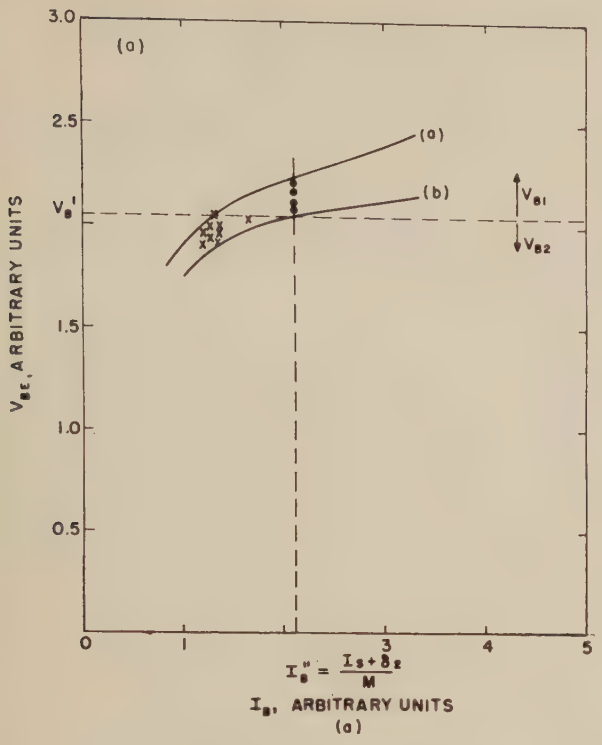

Fig. 12—"On" state specification I—schematic.

siderably less than the decrease of $V_{B\,off}$, which corresponds to a given I_L, and in general does not warrant consideration in the establishment of a specification. Consequently, the "on" state specifications are generally stipulated at room temperature.

Fig. 12 illustrates schematically the first type of specification. If a system parameter M is defined such that

$$I_B'' = \frac{I_S + \delta_2}{M}$$

is the minimum value of base current which the circuit design rules and the transistor specification assure as being available for each "on" transistor, then the minimum voltage appearing on the base of a nominally "on" unit in the system environment is given by

$$V_{B1} = V_{BE}\left(I_C = I_S + \delta_2, I_B = \frac{I_S + \delta_2}{M}\right). \qquad (23)$$

Values of V_{B1} for a schematic representation of base input characteristics similar to that of Fig. 10 are shown as dots along the line I_B'' of Fig. 12. The maximum base emitter voltage necessary for each transistor to obtain the required $V_{C\,on}$ appropriate to the "on" state can be defined by

$$V_{B2} = V_{BE}(I_C = I_S + \delta_2, V_{CE} = V_{C\,on}). \qquad (24)$$

Values of V_{B2} correspond to the ordinates of the "on" state points marked by the x in Fig. 12. The specification

$$V_{B1} \geq V_{B2} + \Delta' \qquad (25)$$

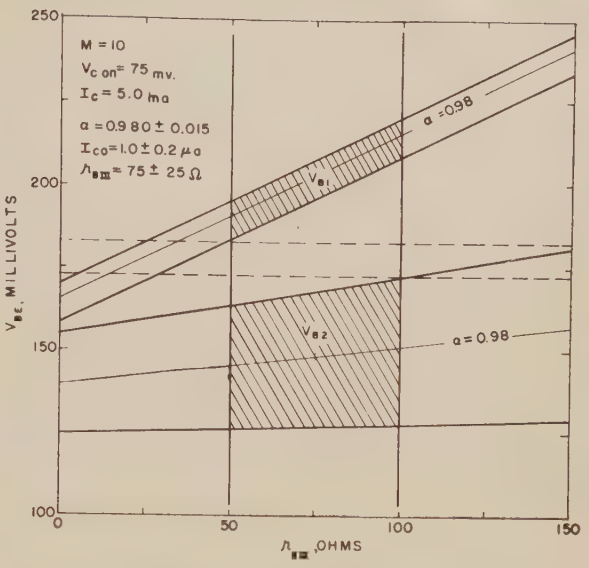

Fig. 13—"On" state specification I—effect of parameter value variations for symmetric transistor.

for all transistors employed in the circuit in conjunction with circuit design rules in the form of N_C, N_B pairs which satisfy a modified form of (1), as given by

$$N_C I_L + N_B\left(\frac{I_S + \delta_2}{M}\right) \leq I_S - \delta_1, \qquad (26)$$

then insures that all units exhibit a value of β^* and a base-input characteristic which is both of sufficient slope and of suitable orientation to the input characteristics of all other transistors that it may be base-connected at the same node. The quantity Δ' is a base-emitter voltage margin, included to allow for spurious signals which tend to increase the unbalance of "on" unit base currents, and was introduced in Section II. Within a limited range both those units exhibiting a low β^* but an input characteristic which provides greater than average I_{Bj}, and those units exhibiting a high β^* but an input characteristic which provides less than average I_{Bj}, can satisfy the specification.

The voltages V_{B1} and V_{B2} can be expressed in terms of fundamental parameters by the methods employed previously. In Fig. 13 the zones of possible values of V_{B1} and V_{B2} are shown in the V_{BE}-r_{bIII} plane for a hypothetical case of a symmetric transistor ($\alpha_N = \alpha_I$). It is assumed that I_{CO}, α, and r_{bIII} are independent in order to give a semiquantitative description of the relative effects of average parameter values and their variations on the satisfaction of the specification. A decrease in the average α causes the zones to close together by a downward translation of the V_{B1} zone and by a more marked upward translation and counter-clockwise rotation of the V_{B2} zone. If a sufficient decrease in average α occurs, the condition $V_{B1} \geq V_{B2}$ may not be satisfied for all transistors. An increase in the variation of α results in a broadening of the zones. Similar results are obtained for a decrease in the average value and an increase in the variation of r_{bIII}. An increase in the

variation of I_{CO} broadens the zones in the vertical direction. However, a change in the mean value of I_{CO} effects only the magnitude of $V_{B\ on}$, therefore the only effect on the "on" state is in the current regulation term δ_1. The "off" state, of course, is directly affected.

Fig. 14 illustrates schematically the second type of specification. The indicated slope of the V_{BE}-I_B envelope is considerably less in this case as it is applicable to those transistor types for which r_{bIII}, α_I, or both are of small magnitude [see (17)]. In this specification it is assumed that the limitation on base current variation is effected by a single value of external base resistor for each transistor. The specification is in two parts of which the first is a lower limit on β^*, which is denoted by G, in the form

$$V_{CE}\left(I_C = I_S + \delta_2, I_B = \frac{I_S + \delta_2}{G}\right) \leq V_{C\ on}, \qquad (27)$$

and the second is a restriction on the variation of V_{BE} at the same value of G, or

$$V_{BE}^{**} \leq V_{BE}\left(I_C = I_S + \delta_2, I_B = \frac{I_S + \delta_2}{G}\right) \leq V_{BE}^{**}. \qquad (28)$$

The spread of base currents I_{Bj}, which is permitted by the transistor specification and the circuit design, depends then on the value and maximum variation of the external base resistor $R \pm \delta R$ and the sum of the base voltage variation allowed by the specification plus the spurious signal margin.

$$\delta\Phi = V_{BE}^{*} - V_{BE}^{**} + \Delta'. \qquad (29)$$

If the current available to the N_B bases is denoted by I^*,

$$I^* = I_S - \delta_1 - N_C I_L. \qquad (30)$$

Then

$$N_B = \frac{\left(I^* - \dfrac{I_S + \delta_2}{G}\right)(R - \delta R)}{\left(\dfrac{I_S + \delta_2}{G}\right)(R + \delta R) + \delta\Phi} + 1. \qquad (31)$$

This expression is based on the assumption that Φ_E is independent of I_B. For a positive input resistance this approximation yields a conservative value for N_B.

There is no unique procedure in the adjustment of specification values to the observed behavior of a given transistor type. An approach which permits a rapid adjustment of specification values is to start with an initial trial value of I_L for the desired maximum operating temperature. Examination of a family of I_C-V_{BE} curves similar to those of Fig. 1, except for temperature of measurement, then gives a value of $V_{B\ off}$. With this

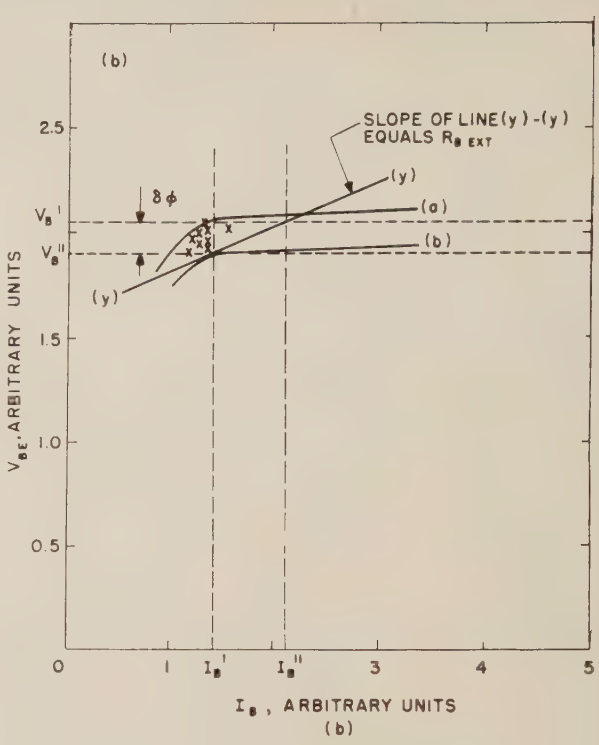

Fig. 14—"On" state specification II—schematic.

value of $V_{B\ off}$ a value for I_L' of (25) can be determined, and the subtraction of the value of Δ to be included in the system design yields $V_{C\ on}$. An examination of a family of V_{CE}-I_B curves similar to Fig. 2 will indicate an appropriate value for β^*, and a family of V_{BE}-I_B curves similar to Fig. 4 indicates the type of specification which may be applicable. For the second type of "on" state specification, a minimum value of β^*, G can be set directly from the V_{CE}-I_B curves, and appropriate limits for the variation of V_{BE} can be determined from the V_{BE}-I_B curves. Since the first type of specification admits of some compensation between β^* and the input characteristics, a value of β^*, somewhat higher than that of the first type of specification, can be considered in conjunction with the observed spread in base current values at a given base potential to determine a value of M. A readjustment of the initial trial value of I_L may, of course, be required or be advantageous at some point in the process. The process is roughly cyclic and, rather than I_L, the initial point might be β^*. The former is perhaps best applied to germanium transistors for which I_L is more likely to be limiting and the latter for present-day silicon transistors for which β^* tends to be the limiting quantity.

VII. Acknowledgment

The author wishes to acknowledge the comments and criticisms of J. R. Harris, which have considerably influenced the preparation of this material.

An Analysis of Certain Errors in Electronic Differential Analyzers II—Capacitor Dielectric Absorption*

PAUL C. DOW, JR.†

Summary—The permittivity or dielectric constant of the materials used in capacitors is not actually a constant but is a complex function of frequency and temperature. Consequently, the feedback capacitors used in the integrators of a differential analyzer cannot be considered ideal, but their capacitance must be considered a variable. Methods of representing the complex capacitance are discussed and a model is selected which is conveniently suited to the analysis. Experimental methods of measuring the complex capacitance are described. The phenomenon of dielectric absorption is interpreted in terms of the capacitor model and it is shown that an integrator having such a feedback capacitor will experience a change in effective initial conditions after a solution is started on the computer. It is also shown that when such integrators are used to solve linear differential equations with constant coefficients, the locations of the roots of the characteristic equation are changed slightly; these changes can be evaluated when the properties of the capacitor model are known.

Introduction

A well-known phenomenon exhibited by dielectric materials is that of dielectric absorption.[1] When a potential difference is applied to a dielectric, the polarization current or charging current consists of two distinct types. The first is the charging current which occurs practically instantaneously; the second is that which occurs more slowly during a measurable period of time. The former is caused by the rapidly forming, or instantaneous, electronic and atomic polarizations. The latter is caused by slowly forming, or absorptive, dipole and interfacial polarizations. Only the interfacial polarizations have relaxation times which are large enough to be of interest in analog computer applications. (The relaxation time is a quantitative measure of the time required for a polarization to form or disappear.)

The theory of dipole polarizations as developed by Debye[2] shows that the dielectric constant can be considered a complex function defined by

$$\epsilon^* = \epsilon' - j\epsilon''. \tag{1}$$

When expressed in terms of frequency and relaxation time, the complex dielectric constant becomes

$$\epsilon^* = \epsilon_\infty + \frac{\epsilon_0 - \epsilon_\infty}{1 + j\omega\tau_0} \tag{2}$$

where ϵ_0 is the zero frequency or static dielectric constant, ϵ_∞ is the infinite frequency dielectric constant, and τ_0 is the relaxation time which is a function of temperature.

The theory of interfacial polarizations has been treated by several writers,[3–7] and various expressions for the complex dielectric constant have resulted, all determined in part by empirical parameters. Of these, perhaps the simplest is that proposed by Cole and Cole,[7] which is

$$\epsilon^* = \epsilon_\infty + \frac{\epsilon_0 - \epsilon_\infty}{1 + (j\omega\tau_0)^{1-\alpha}} \tag{3}$$

where α is an empirical constant with values from 0 to 1, a measure of the distribution of relaxation times.

Unfortunately, none of these expressions, nor the physical model of the capacitor resulting from them, is particularly well suited to the analysis of the effect of such a capacitor when used as the feedback path of a high-gain amplifier, *i.e.*, when used in an integrator of a differential analyzer. Furthermore, these expressions were based on the results of experiments performed on dielectric materials not commonly used in the capacitors used in analog computers. Consequently, the experiments described below were carried out for two purposes: 1) to develop a useful mathematical expression for the complex capacitance and a physical model for the capacitor, and 2) to evaluate the necessary empirical parameters for a dielectric material commonly employed in precision computer capacitors, namely, polystyrene.

Transient Current Measurements

For the measurement of the charging current, an electrometer was connected in series with the capacitor and a battery. The charge on the electrometer was re-

* Manuscript received by the PGEC, July 17, 1957. This paper contains part of the results of a dissertation submitted by the author in partial fulfillment of the requirements for the Ph.D. degree at the University of Michigan, Ann Arbor, Mich.

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[1] E. J. Murphy and S. O. Morgan, "The dielectric properties of insulating materials," *Bell Sys. Tech. J.*, vol. 16, pp. 493–512; October, 1937.

[2] P. Debye, "Polar Molecules," Chemical Catalog Company, New York, p. 94; 1929.

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[5] W. A. Yager, "The distribution of relaxation times in typical dielectrics," *Physics*, vol. 7, pp. 434–450; December, 1936.

[6] R. M. Fuoss and J. G. Kirkwood," Electrical properties of solids, VIII," *J. Amer. Chem. Soc.*, vol. 63, pp. 385–394; February, 1941.

[7] K. S. Cole and R. H. Cole, "Dispersion and absorption in dielectrics—I. Alternating current characteristics," *J. Chem. Phys.*, vol. 9, pp. 341–351; April, 1941.

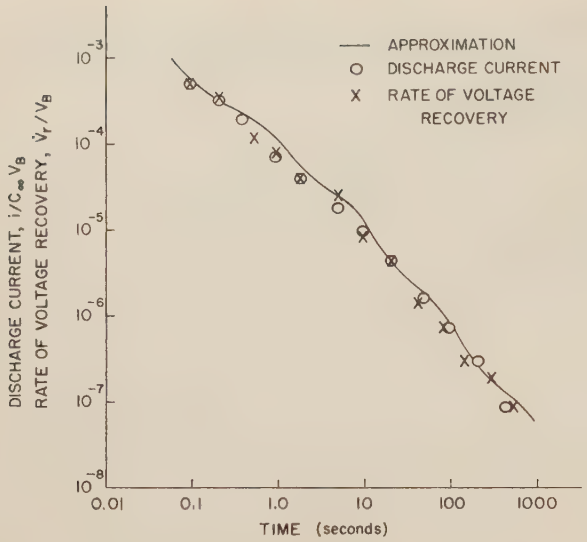

Fig. 1—Capacitor discharge current and rate of voltage recovery.

corded, and its rate of change evaluated to give the current. The discharge current was measured in a similar manner by replacing the battery by a short circuit. The charging current was influenced by the capacitor leakage resistance and by the battery voltage recovery following the initial surge of current. Since the discharge current was not subject to these influences, the charging current will not be considered in what follows.

It was noted that, due to the dielectric absorption effect, the magnitude of the discharge current depended on how long the capacitor was charged prior to being discharged. If the capacitor was charged for more than fifteen minutes, the discharge current during the period of observation (about five minutes) stabilized and did not change when a longer charging interval was used.

The data points in Fig. 1 show the measured discharge current for a 1-μf polystyrene capacitor following a fifteen-minute charging interval. Initial charging voltages of from 23 to 110 volts were used with results essentially identical to those shown in Fig. 1. No difference in results was noted for temperatures ranging from 66°F to 102°F.

Any number of functions could be selected to fit the data in Fig. 1. The function selected was

$$\frac{i}{C_\infty V_B} = \sum_k a_k e^{-t/T_k} \tag{4}$$

where the number of terms would be determined by the accuracy required in the approximation.

In Fig. 2 the current i, following the application of voltage V_B with the capacitors initially discharged, is given by

$$\frac{i}{C_\infty V_B} = \sum_k \frac{1}{R_k C_\infty} e^{-t/R_k C_k}. \tag{5}$$

The discharge current which would flow if the terminals in Fig. 2 were shorted after all the capacitors are

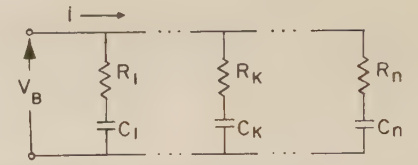

Fig. 2 —Model of absorptive portion of capacitor.

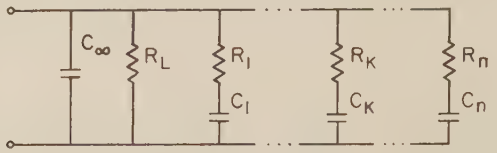

Fig. 3—Model of capacitor based on experimental results.

charged to V_B volts is, of course, also given by (5). Eqs. (4) and (5) will be the same if the resistors and capacitors have values given by the following relations:

$$R_k C_\infty = \frac{1}{a_k}$$
$$\frac{C_k}{C_\infty} = T_k a_k. \tag{6}$$

It follows directly then that the equivalent circuit for the capacitor is as shown in Fig. 3, where the leakage resistance R_L is included. A similar model has also been suggested by Single.[8]

It is possible, using five resistor-capacitor combinations, to fit the data given in Fig. 1 if the values used for the components in Fig. 3 are those given in Table I. The discharge current which would result from this approximation is plotted in Fig. 1 for comparison with the experimentally observed discharge current.

TABLE I
EXPERIMENTAL VALUES FOR CAPACITOR MODEL

k	C_k/C_∞	$R_k C_\infty$ (seconds)	$T_k = R_k C_k$ (seconds)
1	1.40×10^{-4}	3.56×10^{6}	500
2	2.00×10^{-4}	2.50×10^{5}	50
3	2.70×10^{-4}	2.00×10^{4}	5.4
4	1.93×10^{-4}	3.03×10^{3}	0.585
5	1.20×10^{-4}	3.34×10^{2}	0.040

$R_L C_\infty = 5.0\times10^{6}$

COMPLEX CAPACITANCE

The complex capacitance C^* of the model in Fig. 3 can be evaluated from its admittance since, for a capacitor,

$$Y(j\omega) = j\omega C^*. \tag{7}$$

From Fig. 3, the admittance is seen to be

$$Y(j\omega) = j\omega C_\infty + \sum_k \frac{1}{R_k + \dfrac{1}{j\omega C_k}} \tag{8}$$

[8] C. H. Single, "Precision Components for Analog Computers," paper presented at ISA Convention, New York, N. Y.; 1956.

where the admittance due to the leakage resistance is not included since it is not part of the polarization process.

The complex capacitance from (7) and (8) is

$$C^*(j\omega) = C_\infty + \sum_k \frac{C_k}{1 + j\omega T_k} \tag{9}$$

where T_k is the kth relaxation time, R_kC_k. From (9) it is clear that the infinite frequency capacitance is

$$C_\infty = C^*]_{\omega=\infty} \tag{10}$$

and the zero frequency capacitance is

$$C_0 = C^*]_{\omega=0} = C_\infty + \sum_k C_k. \tag{11}$$

The complex capacitance can also be expressed in terms of its real and imaginary parts as

$$C^* = C' - jC'' \tag{12}$$

where

$$C' = C_\infty + \sum_k \frac{C_k}{1 + \omega^2 T_k^2} \tag{13}$$

$$C'' = \sum_k \frac{\omega C_k T_k}{1 + \omega^2 T_k^2}. \tag{14}$$

If C^* is expressed in polar coordinates, one has

$$C^* = |C^*| e^{-j\delta} \tag{15}$$

where

$$|C^*| = \sqrt{C'^2 + C''^2} \tag{16}$$

$$\tan \delta = \frac{C''}{C'}. \tag{17}$$

Tan δ is the loss tangent or dissipation factor of the dielectric. If $\sum_k C_k \ll C_\infty$, the following approximate expressions can be derived:

$$|C^*| = C_\infty + \sum_k \frac{C_k}{1 + \omega^2 T_k^2} \tag{18}$$

$$\delta = \frac{1}{C_\infty} \sum_k \frac{\omega C_k T_k}{1 + \omega^2 T_k^2}. \tag{19}$$

Eq. (19) is plotted in Fig. 4 in dashed lines for the capacitor model given by Table I.

Cole and Cole, in a second paper,[9] have evaluated the transient current following the application of a constant voltage to a capacitor having a dielectric constant given by (3). These results can be made to agree with the experimental discharge current of Fig. 1 if the parameters have the following values:

[9] K. S. Cole and R. H. Cole, "Dispersion and absorption in dielectrics—II. Direct current characteristics," *J. Chem. Phys.*, vol. 10, pp. 98–105; February, 1942.

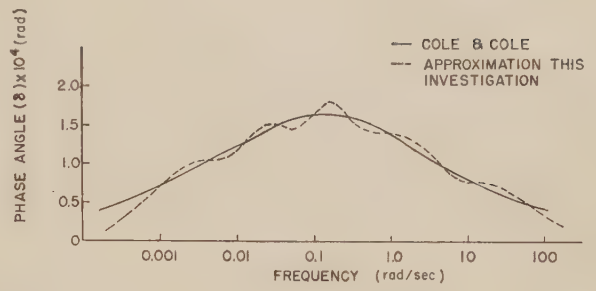

Fig. 4—Phase angle of the complex capacitance vs frequency.

$$\alpha = 0.6$$

$$\tau_0 = 7.0 \text{ seconds}$$

$$\frac{C_0 - C_\infty}{C_\infty} = 10^{-3}. \tag{20}$$

The details of the method used for matching the transient current curves are given by Field.[10]

The value of the dissipation factor, δ, as given by Cole and Cole[9] using the parameters given in (20) is plotted in Fig. 4 in a solid line for comparison with (19). Although the method of Cole and Cole permits the complex capacitance to be described by fewer parameters than does the method used here, the latter method lends itself more readily to the error analysis which is the purpose of this report.

Capacitor Voltage Recovery

If a capacitor is charged at a constant voltage for a period of time and then briefly discharged by short circuiting its terminals, a voltage is observed to build up on the open-circuited terminals due to the slow forming polarizations. This behavior provides a convenient means of measuring the same properties of the dielectric which were determined by the transient current measurements described above.

If the model of the capacitor in Fig. 3 is charged with a voltage V_B for a length of time, which is long compared to the longest relaxation time R_kC_k, then each of the capacitors C_k will be charged to essentially V_B volts. The voltage V_B is removed and the capacitor terminals are short-circuited for a length of time, which is short compared to the shortest relaxation time, thus reducing the voltage on C_∞ to zero and leaving the voltage on the other capacitors still essentially at V_B. The short circuit is removed and the capacitor terminals are left open-circuited. A time varying voltage will now appear on the terminals. Let this recovery voltage be defined as V_r.

If the leakage resistance R_L is large enough for a negligible portion of the charge on C_∞ to leak off during the voltage recovery (*i.e.*, if $R_LC_\infty \gg R_kC_k$) and if, in

[10] R. F. Field, "Dielectric Measuring Techniques, Permittivity, Lumped Circuits" in "Dielectric Materials and Applications," A. R. von Hippel, ed., John Wiley and Sons, New York, N. Y., pp. 47–62; 1954.

addition, $C_k/C_\infty \ll 1$, analysis of Fig. 3 gives for the recovery voltage

$$V_r \cong \frac{V_B}{C_\infty} \sum_k C_k(1 - e^{-t/R_kC_k}). \tag{21}$$

Differentiating (21) with respect to time and rearranging yields

$$\frac{\dot{V}_r}{V_B} = \sum_k \frac{1}{R_kC_\infty} e^{-t/R_kC_k}. \tag{22}$$

Comparison of (5) and (22) shows that

$$\frac{\dot{V}_r}{V_B} = \frac{i}{C_\infty V_B} \tag{23}$$

where V_r is the recovery voltage and i is the discharge current. Thus the measurement of the capacitor recovery voltage can be used to obtain the same information as that obtained from current discharge measurements.

The recovery voltage can be measured by connecting the capacitor to a very high impedance voltmeter, such as an electrometer. An alternative method is to use the capacitor as the feedback of a high-gain computer amplifier. With the computer in the operating condition, the capacitor is discharged by short-circuiting its terminals. The build-up of voltage on the capacitor will then appear as the output voltage of the high-gain amplifier. The advantage of this method is that the capacitor characteristics can be determined without removing it from the computer and without additional equipment. A disadvantage is the integrator drift due to grid current. This effect can be minimized, however, by making two tests using the same amplifier, the second test with the charging voltage equal in magnitude but opposite in sign to the first. When the results of the two tests are subtracted, the integrator drift will be eliminated.

Results of a typical experimental measurement of the voltage recovery, using the same polystyrene capacitor as before, are shown in Fig. 1.

Integrator Errors

Fig. 5 shows a high-gain operational amplifier connected as an integrator with a feedback capacitor having dielectric absorption represented by the model developed earlier. Assuming that the amplifier is ideal[11] (*i.e.*, it has infinite gain), the following equations can be written:

$$i_i = i_c + \sum_k i_k \tag{24}$$

$$i_i = \frac{V_i}{R_i} \tag{25}$$

[11] For a discussion of the effect of nonideal amplifiers see P. C. Dow, Jr., "An analysis of certain errors in electronic differential analyzers—I. Bandwidth limitations," IRE Trans. on Electronic Computers, vol. EC-6, pp. 255–260; December, 1957.

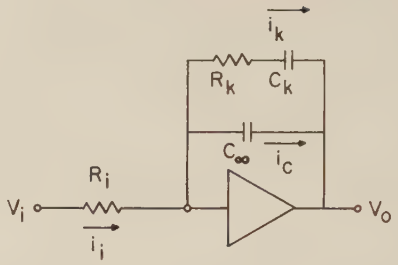

Fig. 5—Amplifier connected as an integrator.

$$i_c = -C_\infty \frac{dV_0}{dt} \tag{26}$$

$$R_k \frac{di_k}{dt} + \frac{i_k}{C_k} = -\frac{dV_0}{dt}. \tag{27}$$

Taking the Laplace transform of (24)–(27) and eliminating the current terms yields

$$\left[C_\infty + \sum_k \frac{C_k}{R_kC_ks + 1}\right][sV_0(s) - V_0(0)] = -\frac{V_i(s)}{R_i} + \sum_k \frac{R_kC_ki_k(0)}{R_kC_ks + 1} \tag{28}$$

where

$$V_0(s) = \mathcal{L}[V_0(t)]$$
$$V_0(0) = V_0(t)]_{t=0}. \tag{29}$$

Making use of (9) in (28) gives

$$V_0(s) = -\frac{V_i(s)}{sR_iC^*(s)} + \frac{V_0(0)}{s} + \frac{1}{sC^*(s)} \sum_k \frac{R_kC_ki_k(0)}{R_kC_ks + 1}. \tag{30}$$

The first term in (30) will give the output of the integrator resulting from a given input; the second and third terms give the output resulting from the initial conditions.

Consider the response of the integrator to a unit impulse. If $R_iC_\infty = 1$, the first term of (30) becomes

$$V_0(s) = -\frac{1}{s\left[1 + \sum_k \frac{C_k/C_\infty}{1 + T_ks}\right]}. \tag{31}$$

If $\sum_k C_k/C_\infty \ll 1$, (31) can be written approximately as

$$V_0(s) = -\frac{1}{s}\left[1 - \sum_k \frac{C_k/C_\infty}{T_ks + 1}\right]. \tag{32}$$

Taking the inverse Laplace transform of (32) yields

$$V_0(t) = -1 + \sum_k \frac{C_k}{C_\infty}(1 - e^{-t/T_k}). \tag{33}$$

The last term of (33) is the voltage recovery to a unit applied voltage, as given by (21). Then (33) can be written

$$V_0(t) = -1 + \frac{V_r(t)}{V_B} \tag{34}$$

where $V_r(t)$ is the recovery voltage following an applied voltage V_B.

That is, the effect of dielectric absorption is to reduce the magnitude of the desired integrator impulse response by the amount of the capacitor voltage recovery.

Similarly, it can be shown that if

$$V_i(t) = R_i C_\infty \cos \omega t, \tag{35}$$

the integrator output is approximately

$$V_0(t) = -\frac{C_\infty}{\omega |C^*|} \sin(\omega t + \delta) \tag{36}$$

where $|C^*|$ and δ are defined by (18) and (19).

The second term in (30) is the normal initial condition of the integrator. The third term produces an effective change in initial conditions. This can be seen as follows. If the initial condition voltage $V_0(0)$ is applied to the integrating capacitor in Fig. 5 for a very short time so that the capacitors C_k representing the dielectric absorption remain uncharged, then

$$i_k(0) = -\frac{V_0(0)}{R_k}, \tag{37}$$

and the integrator output due to the last two terms in (30) becomes

$$V_0(s) = \frac{V_0(0)}{s}\left(1 - \sum_k \frac{C_k/C_\infty}{R_k C_k s + 1}\right) \tag{38}$$

where C^* has been set equal to C_∞ in the last term since doing so will be ignoring second-order error terms. Taking the inverse transformation of (38) yields

$$V_0(t) = V_0(0)\left[1 - \frac{V_r(t)}{V_B}\right] \tag{39}$$

where $V_r(t)$ is the recovery voltage following an applied voltage V_B. If the capacitors C_k are initially charged from a previous operation or by applying the initial conditions for a longer time, the recovery voltage will be different from that defined by (21). This effective change in initial conditions would be of particular significance in high-speed repetitive computers where high accuracy is required and where the initial conditions must be reset in minimum time. It would also be important for boundary value problems in which the solution depends critically on the initial, or boundary, conditions.

Errors in Solutions of Equations

Let the computer be set up to solve a differential equation described by the characteristic equation

$$C\{s\} = 0. \tag{40}$$

If only integrators and summers are used and if each integrator output is described by (30), it is clear that the operator s in the given characteristic equation will be replaced by $sC^*(s)/C_\infty$. That is, the characteristic equation solved by the computer will be

$$C\left\{s\frac{C^*(s)}{C_\infty}\right\} = 0. \tag{41}$$

Then, if s_i is a root of (40) and s_i' is a root of (41),

$$s_i = s_i' \frac{C^*(s_i')}{C_\infty}. \tag{42}$$

Let the roots of the computer solution be given by

$$s_i' = s_i + e_i \tag{43}$$

where e_i is the error in the root s_i. Substituting (43) in (42) yields

$$e_i \cong -s_i \sum_k \frac{C_k/C_\infty}{1 + T_k s_i} \tag{44}$$

where it is assumed that $e_i \ll s_i$. From (44) the errors in the characteristic roots can be evaluated if the roots of the given equation and the capacitor dielectric properties are known.

Example of Simple Harmonic Motion

As an example of the computer error produced by dielectric absorption, consider the equation of simple harmonic motion:

$$\ddot{x} + \omega^2 x = 0. \tag{45}$$

The roots of the characteristic equation are

$$s_i = \pm j\omega. \tag{46}$$

From (44), (43), and (19), the roots of the computer solution are

$$s_i' = -\omega\delta \pm j\omega\left(1 - \sum_k \frac{C_k/C_\infty}{1 + \omega^2 T_k^2}\right). \tag{47}$$

Thus the dielectric absorption introduces damping in the solution and changes the frequency of oscillation. The damping ratio resulting from dielectric absorption is a function of frequency and is approximately

$$\zeta = \delta(\omega). \tag{48}$$

It was shown in an earlier article[11] that, if the computer is set up as shown in Fig. 6, the damping ratio introduced by computer bandwidth limitations is

$$\zeta = \frac{1}{\omega T_1} - \frac{\omega(T_s + 2T_2)}{2} \tag{49}$$

where T_1 and T_2 are time constants determined by the integrator characteristics and T_s is the time constant determined by the summer characteristics. The total damping ratio is the sum of (48) and (49).

Experimental Results

To compare the theoretical damping ratio given by (48) and (49) with that obtained experimentally, the Sterling Electronic Differential Analyzer[12] was used. The computer was set up as shown in Fig. 6. The capacitors used in the integrators were the type for which experimental values were given in Table I. The integrator and summer time constants were determined by using the methods given in the previous article[11] and were

$$\frac{1}{T_1} = 5.2 \times 10^{-6}$$

$$T_2 = 2.0 \times 10^{-7}$$

$$T_s = 2.0(1 + \omega^2) \times 10^{-7}. \tag{50}$$

Fig. 6—Computer setup for simple harmonic motion.

The theoretical damping ratio vs frequency is shown in Fig. 7, and the portion due to dielectric absorption only is indicated. The experimentally observed damping ratio is plotted in Fig. 7 and shows very good agreement with the predicted values.

[12] Model LM-10, Sterling Instruments Co., Detroit, Mich.

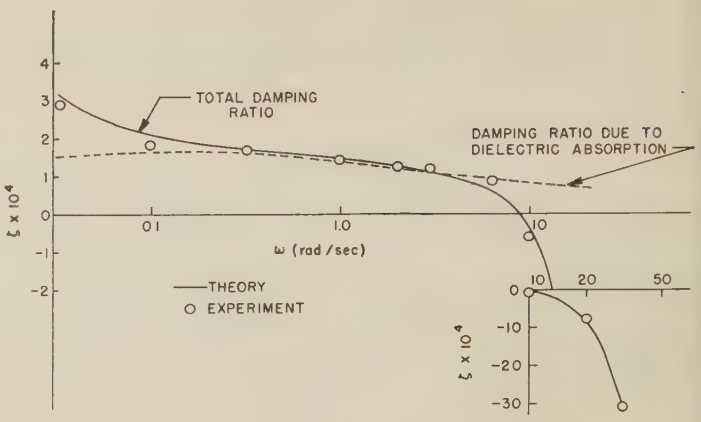

Fig. 7—Damping ratio introduced by the computer.

It will be noted that, for frequencies between 0.1 and 10 rad/second, the dielectric absorption makes the major contribution to the damping. It is clearly a source of error which must not be overlooked when considering the accuracy of differential analyzers, especially at low frequencies.

Acknowledgment

The author is grateful to R. M. Howe, the chairman of his doctoral committee, for his continued advice and counsel, and to R. F. Field for his helpful explanations of previous work on dielectric materials. He is indebted to the United States Air Force for providing him with the opportunity and facilities to pursue this investigation while associated with the Air Force Institute of Technology.

A Study of Refill Phenomena in Williams' Tube Memories*

J. M. MAUGHMER† AND H. D. HUSKEY‡

Summary—A dot-circle scheme is proposed which will permit the distinction between binary "0" and "1" signals when the stored information has been destroyed approximately 90 per cent by refill. This unusual recovery of stored information is accomplished by making proper choices of operating parameters and using discharging effects instead of the charging effects as has been done in the past.

Basic relationships are developed from Coulomb's law and the equivalent circuit of the Williams' memory to predict the binary output signals. The agreement between these theoretical signals and the actual experimental signals is remarkably good. A 5JP11 cathode-ray tube was used in the experimental work.

I. Introduction

THIS PAPER proposes a dot-circle storage scheme along with theoretical and experimental results which show close agreement. The dot-circle system presented is an expansion of an idea introduced by Thorensen[1] using a dot-dash system. Thorensen's idea is to delay the examination of the Williams' Tube output signal until all charging effects have disappeared. Charging of the spot will occur at readout time when the spot under examination is not fully charged to its equilibrium positive potential. The reading beam will immediately charge the spot to the equilibrium potential and through capacitive coupling this positive charging will appear as part of the Williams' Tube output signal. By delaying the examination of the output signal, only effects due to discharging will remain. Thorensen has shown that the later portion of the output signal which is due to discharging is nearly independent of the initial refill conditions.

The discharging effects in a dot-dash system using a dot-read method are due to partial destruction of the dash by the reading dot. Secondary electrons emitted from the spot are attracted to the positive region of the dash, thereby partially destroying the dash. This discharge is capacitively coupled to the Williams' Tube output and appears in the output signal. The magnitude of the output signal during charging is much greater than during the discharging portion.

The reason for choosing the dot-circle scheme is to enhance the discharging effects used by Thorensen in the improvement of his dot-dash system. The basic idea of using a circle instead of a dash is that a circle will provide approximately five times more discharging area in the immediate vicinity of the dot than a dash and therefore give a greater magnitude to the discharging portion of the output signal.

The time constant for charging a spot on the phosphor surface to its equilibrium potential is approximately 0.3 μsec. Charging of the surface contributes a positive component to the output signal. Discharging, on the other hand, causes a negative component to appear in the output signals. Discharging effects have a time constant in the order of 9 μsec. Thus the discharging effects last much longer.

The circle diameter must be large enough to provide sufficient discharging area but not so large that a dot written in its center is unable to eradicate the stored circle. Any residual left by the circle will affect the next reading at that spot, tending to make the output signal more negative than it should be. The circle diameter that proved to be most satisfactory in the experimental system was approximately 0.058 inch in outer diameter whereas the dot itself was approximately 0.040 inch in diameter. The circle appeared as a larger dot since the focused beam with which the circle was written was 0.040 inch.

The circle size is not the only important parameter. The peak beam current, the unblanking duration, and the input resistance to the amplifier play important roles in establishing a satisfactory system. The frequency of circle generation has little or no effect on the final output signals. The only frequency requirement is that it be high enough to allow one complete circle to be traversed during unblanking time. Frequencies ranging from 1 to 10 mc were tried. The results shown in pictorial form are for waveforms using circle frequencies of 2 and 6 mc.

The peak beam current has an optimum value. It cannot be too small or else the distinction between output signals disappears. If it is too large, too many secondary electrons are liberated causing excessive destruction of neighboring bits of stored information. The most satisfactory peak beam current was found to be in the range of 6.5 to 7.0 μamp.

It is vital that a dot written in the center of a previously stored circle destroys the circle as much as possible. This destruction is accomplished most effectively by holding the dot in position from 4 to 6 μsec. The ring of charge built up by the circle is approximately constant whether the circle is traversed once or twenty times. The unblanking time must be held as short as

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[1] R. Thorensen, "An Improved Cathode Ray Tube Storage System," Natl. Bureau of Standards, Washington, D. C., Rep. 2275; February 6, 1953.

possible; however, in order to reduce the number of secondaries spreading out to neighboring spots, the unblanking time found to be most favorable was 4.5 μsec.

The input resistance to the high-gain amplifier determines the basic characteristics of the output waveforms. With a large resistance, the time constants are such that the input signals to the amplifier have an extended duration. As the input resistance is reduced the signals have less magnitude and shorter time constants. Input resistance ranging from 28 kilohms to 1 megohm were tried.

In the course of this experimental work, unblanking frequencies were varied from one pulse per second up to sixty thousand pulses per second. The change in amplitude of the output waveforms was negligible in this range. For convenience then, the results shown later in pictorial form were taken with an unblanking frequency of ten thousand pulses per second.

Section II describes the experimental work using just two dots. Two basic equations are derived and compared with experimental results. One is an equation describing how refill changes the neighboring spots. The other is an equation derived from an equivalent circuit of the Williams' Tube output mechanism which gives the expression for the output waveforms of a dot reading a dot for different degrees of refill. It agrees remarkably well with experimental results.

Section III shows how the dot-circle storage system can be used to reclaim stored information which had been nearly destroyed by refill. The equations from Section II are expanded to give a new equation that again shows remarkable agreement with experimental results for dot-reading-a-circle waveforms with various degrees of refill.

II. Dot-Reading-Dot Experiments

This section pertains to an investigation of the refill effects on one spot while the electron beam impinges on a neighboring spot. One dot is referred to as the reference dot or spot 1. The other is referred to as the deflected dot or spot 2. The separation between the two dots is controlled manually. The deflection circuitry is arranged so that spot 1 can be bombarded n times before spot 2 is examined. The number n is controlled by a pulse scaler. By varying the spot separation and the number of times spot 1 is bombarded, it is possible to determine how spot 2 is effected by refill.

Development of the Refill Equation

The refill equation

$$Y = \left[1 - \exp - \frac{k[A_s - A_0]n}{(s-d)^2}\right] \times 100 \qquad (1)$$

describes the percentage change in output waveforms for a dot reading a dot in terms of spot separation, spot area, and the number of bombardments in the vicinity of the test spot. The general form of this expression is developed by using Coulomb's law of attraction. The final relationship between the parameters is determined by experiment.

Y is the percentage change in the output waveforms. This percentage is based on the difference between waveforms obtained with no refill present and for a complete refill of spot 2 (the test spot under observation). A_s is the area of spot 1 or spot 2. A_0 is the area of overlap between spots 1 and 2 if overlap exists. s is the center-to-center separation of the two dots; d is the spot diameter. n is the number of times spot 1 is bombarded by the electron beam before spot 2 is examined. k is a constant, determined to be 0.0013 for the results shown.

The number of secondary electrons emitted from spot 1 that will be captured by spot 2 will depend upon the attractive force F of spot 2. From Coulomb's law of attraction,

$$F \propto \frac{q}{D^2}, \qquad (2)$$

where q is the positive charge at spot 2 and D is the separation between spots 1 and 2. As the charged spot captures more secondaries, its attractive force will decay. The rate of change of charge at spot 2 is proportional to its attractive force

$$\frac{dq}{dt} \propto -\frac{q}{D^2}. \qquad (3)$$

Since n represents the number of bombardments each of which is an increment of time, then letting $t = nT$ where T is the unblanking time,

$$\frac{dq}{dn} \propto -\frac{Tq}{D^2} \quad \text{or} \quad \frac{dq}{dn} = -\frac{Kq}{D^2} \qquad (4)$$

where K is a constant of proportionality. Integrating (4) with the initial conditions that $q = q_0$ when $n = 0$, one obtains

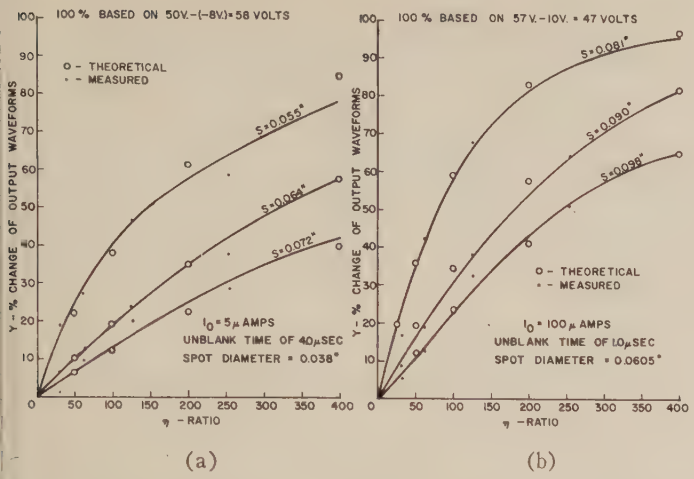
$$q = q_0 e^{-Kn/D^2} \qquad (5)$$

where q_0 is the equilibrium positive charge on spot 2. The percentage change in charge at spot 2 at the time of its bombardment is then

$$Y = \text{per cent change} = \frac{q_0 - q_0 e^{-Kn/D^2}}{q_0} \times 100$$
$$= (1 - e^{-Kn/D^2}) \times 100 \qquad (6)$$

where K and D are to be determined by experiment. So far, D has been used as the separation between spots but it does not indicate how overlap of spots can be accounted for.

D therefore is modified so that spot diameter d and center-to-center separation s appear in the equation.



(a) (b)

Fig. 1—Bombarding ratio n vs percentage change of output waveforms for different spot separation and peak beam current.

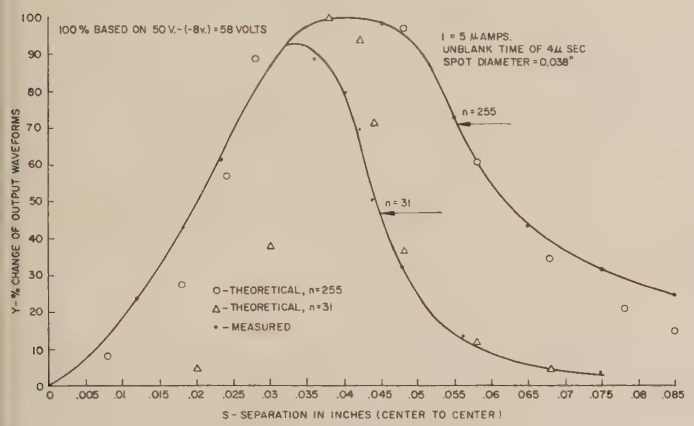


Fig. 2—Spot separation s vs percentage change of output waveforms Y for different bombarding ratios n.

By holding the spot separation s fixed and varying n, the types of curves shown in Fig. 1 are obtained. By holding n fixed and varying s, the types of curves in Fig. 2 are obtained.

The maximum positive output waveforms are obtained when the two spots are adjacent to one another but not overlapping. Under these conditions, the spot separation is just equal to the spot diameter. This provides the information for interpreting D in the expression

$$Y = (1 - e^{-Kn/D^2}) \times 100. \tag{7}$$

D^2 must vanish if Y is to equal 100 per cent when $s=d$, therefore,

$$D^2 = (s - d)^2. \tag{8}$$

As the two spots are made to overlap more and more, Y decreases towards zero. Under these conditions of overlapping, the only portion of spot 2 which can be eradicated is the portion outside spot 1. This suggests that K could vary according to the area of the spots. With K having the units of area, the exponent itself becomes unitless. Using

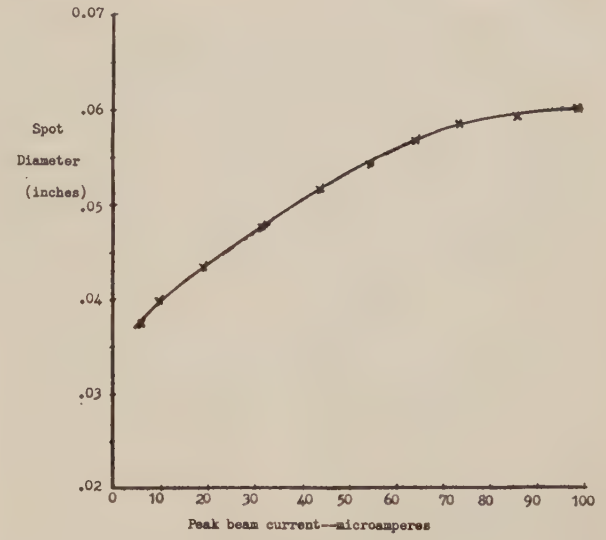


Fig. 3—Variation of spot diameter with peak beam current.

$$Y = \left[1 - \exp - \frac{k\,(\text{area of spot} - \text{area of overlap})\,n}{(\text{separation} - \text{diameter})^2}\right] \times 100 \tag{9}$$

as a starting point, data were taken for different unblanking times and peak currents. By evaluating all the data, it was found that if $k=0.0013$ a best fit between experimental and theoretical curves resulted. Fig. 1 shows the curves for Y vs n comparing the theoretical and measured values. Two extreme cases of peak beam current are shown. In one case the peak beam current is only 5 μamp whereas the other case is for 100 μamp. The curves are drawn to give the best fit of the measured quantities. The maximum n used in the experimental work was 255. The input resistance of the amplifier for the data taken was 100 kilohms.

In Fig. 2, Y is shown plotted against s, the spot separation, while n is held fixed. It can be seen that there is always good agreement between measured and theoretical values when no overlapping of the two spots exists. When overlap does exist, there is still reasonable agreement as long as n is large. The case of greatest interest is, of course, that of no overlap. In a practical storage system the spots will never be allowed to overlap. Fig. 2 not only gives the percentage change of output waveforms, it also gives the percentage change of charge at the spot based on its equilibrium value. For example, with $n=255$ and the separation equal to 0.060 inch, the initial charge at the spot has been reduced to 55 per cent of its equilibrium value.

It was found that the spot diameter varied with peak beam current. For a fixed setting of the focus potentiometer the diameter of the spot increased with an increase in peak beam current as shown in Fig. 3.

Dot-Reading-Dot Waveforms

Here, an expression for the voltage output waveform

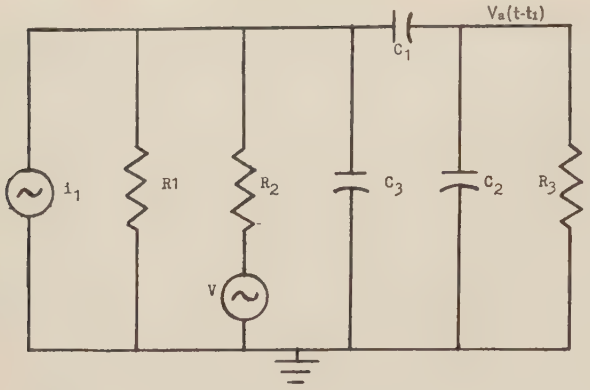


Fig. 4—Equivalent circuit of Williams' Tube.

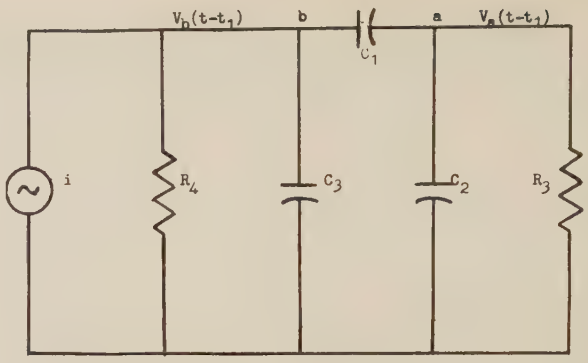


Fig. 5—Simplified equivalent circuit of Williams' Tube.

is developed and compared against photographs of actual output signals.

The equivalent circuit of the Williams' Tube output mechanism is seen in Fig. 4, where

i_1 = the electron beam at the time of unblanking. $= -I_0[U(t-t_1) - U(t-t_2)]$, where $U(t-t_1)=1$, $t>t_1$; $U(t-t_2)=1$, $t>t_2$; $U(t-t_1)=0$, $t<t_1$; $U(t-t_2)=0$, $t<t_2$.

R_1 = resistance between post accelerator and ground.

R_2 = resistance through which the spot charges.

V = voltage generated at the spot.

C_3 = spot capacitance to electrodes other than the pickup plate.

C_1 = spot capacitance to the pickup plate.

C_2 = capacitance to ground of the pickup plate plus the input capacitance to ground at the input of the amplifier.

R_3 = input resistance of the amplifier.

$V_a(t-t_1)$ = voltage appearing at the grid of the amplifier.

If the spot under bombardment is initially discharged, the beam current will charge the spot to an equilibrium potential V_{eq} through R_2 and C_1+C_3. The charging takes place because the secondary emission ratio on the phosphor surface is greater than unity. If the spot is initially at its equilibrium potential, the bombarding beam will not change the potential of the spot. A form of the potential V, which describes this action is

$$V = V_{eq}\left(1 - \exp - \frac{t - t_1}{R_2(C_1 + C_3)}\right) + V_0 \exp - \frac{t - t_1}{R_2(C_1 + C_3)} \tag{10}$$

where V_0 is the initial potential of the spot. The charging current through C_1 due to a change in V is then

$$i = C_1 \frac{dV}{dt} = \frac{C_1(V_{eq} - V_0)}{R_2(C_1 + C_3)} \exp - \frac{t - t_1}{R_2(C_1 + C_3)}. \tag{11}$$

The equivalent circuit of Fig. 4 can now be simplified to that shown in Fig. 5, where

$$i = -I_0[U(t - t_1) - U(t - t_2)] + M \exp - \frac{t - t_1}{R_2(C_1 + C_3)},$$

$$M = \frac{C_1(V_{eq} - V_0)}{R_2(C_1 + C_3)},$$

$$R_4 = \frac{R_1 R_2}{R_1 + R_2}. \tag{12}$$

The problem now is to solve for $V_a(t-t_1)$ using the driving current i of (12). $V_a(t-t_1)$ is the voltage appearing at the grid of the amplifier. If it is assumed that no distortion of the output signal occurs during amplification, $V_a(t-t_1)$ should have the same general features as the actual observed signal at the amplifier output.

The inital conditions at $V_a(t-t_1)$ and $V_b(t-t_1)$ are

$$V_a(0^+) = 0$$

$$V_b(0^+) = -(V_{eq} - V_0). \tag{13}$$

The nodal equations at points a and b of Fig. 5 are

$$(C_1 + C_3)\frac{dV_b(t - t_1)}{dt} + \frac{V_b(t - t_1)}{R_4} - C_1 \frac{dV_a(t - t_1)}{dt} = -I_0[U(t - t_1) - U(t - t_2)] + M \exp - \frac{t - t_1}{R_2(C_1 + C_3)},$$

$$C_1 \frac{dV_b(t - t_1)}{dt} - (C_1 + C_2)\frac{dV_a(t - t_1)}{dt} - \frac{V_a(t - t_1)}{R_3} = 0. \tag{14}$$

Using Laplace transformation techniques, the following expression is obtained for $V_a(t-t_1)$:

$$V_a(t-t_1) = \frac{C_1(V_{eq}-V_0)}{R_4P(s_1-s_2)}U(t-t_1)\left[e^{s_1(t-t_1)} - e^{s_2(t-t_2)}\right]$$
$$- \frac{C_1I_0}{P(s_1-s_2)}\left[U(t-t_1)\left\{e^{s_1(t-t_1)} - e^{s_2(t-t_1)}\right\} - U(t-t_2)\left\{e^{s_1(t-t_2)} - e^{s_2(t-t_2)}\right\}\right]$$
$$+ \frac{C_1M}{P}U(t-t_1)\left[\frac{s_1e^{s_1(t-t_1)}}{(s_1-s_2)\left(s_1+\frac{1}{R_2(C_1+C_3)}\right)} + \frac{s_2e^{s_2(t-t_1)}}{(s_2-s_1)\left(s_2+\frac{1}{R_2(C_1+C_3)}\right)}\right.$$
$$\left. - \frac{\frac{1}{R_2(C_1+C_3)}\exp - \frac{t-t_1}{R_2(C_1+C_3)}}{\left(s_1+\frac{1}{R_2(C_1+C_3)}\right)\left(s_2+\frac{1}{R_2(C_1+C_3)}\right)}\right] \tag{15}$$

where

$$P = C_1C_2 + C_1C_3 + C_2C_3 \tag{16}$$

$$s_1 = -\frac{\left(\frac{C_1+C_3}{R_3P}+\frac{C_1+C_2}{R_4P}\right) + \sqrt{\left(\frac{C_1+C_3}{R_3P}+\frac{C_1+C_2}{R_4P}\right)^2 - \frac{4}{R_3R_4P}}}{2} \tag{17}$$

$$s_2 = -\frac{\left(\frac{C_1+C_3}{R_3P}+\frac{C_1+C_2}{R_4P}\right) - \sqrt{\left(\frac{C_1+C_3}{R_3P}+\frac{C_1+C_2}{R_4P}\right)^2 - \frac{4}{R_3R_4P}}}{2}. \tag{18}$$

By using the following values for the equivalent circuit constants, several plots were made of $V_a(t-t_1)$.

$R_1 = 10^6$ ohms,	$C_1 = 0.1$ $\mu\mu$f,
$R_2 = 3 \times 10^5$ ohms,	$C_2 = 30$ $\mu\mu$f,
$R_3 = 10^5$ ohms.	$C_3 = 1.2$ $\mu\mu$f.

Fig. 6 shows three sets of plotted waveforms, each set having a different unblanking duration. Within each set are three curves representing different initial values of the spot potential at the time of bombardment. Fig. 7 illustrates the actual waveforms under almost the same operating conditions. The initial values of V_0 are slightly different for two of the nine curves that are compared. It can be seen that the theoretical waveforms exhibit all the main characteristics of the actual waveforms.

The values of V_{eq} used in plotting Fig. 6(a)–6(c) were determined by using the actual waveforms of Fig. 7(a)–7(c) as final conditions that must be satisfied by $V_a(t-t_1)$. Take as an example the case shown in Figs. 6(b) and 7(b) where the unblanking time was 1.5 μsec. I_0 was equal to 10 μamp. For the case of $V_0 = V_{eq}$, there was no charging at the spot and all the terms in (15) containing $(V_{eq} - V_0)$ dropped out leaving

$$V_a(t-t_1) = -0.00866[u(t-t_1)\left\{e^{-0.36\times10^6(t-t_1)} - e^{-3.31\times10^6(t-t_1)}\right\} - U(t-t_2)\left\{e^{-0.36\times10^6(t-t_2)} - e^{-3.31\times10^6(t-t_2)}\right\}]. \tag{19}$$

When this equation is plotted, it gives a negative pulse of -0.006 v as seen in Fig. 6(b). This must correspond to the negative pulse in Fig. 7(b) which is -16 v. Now going to the other extreme where $V_0 = 0$ volt, which gives the big positive curve, it can be seen that in the actual waveform of Fig. 7(b) the output signal reaches $+48$ v. The theoretical expression for $V_a(t-t_1)$ from (15) becomes

$$V_a(t-t_1) = [0.00375V_{eq} - 0.00866]U(t-t_1) \cdot \left\{e^{-0.36\times10^6(t-t_1)} - e^{-3.31\times10^6(t-t_1)}\right\}$$
$$+ 0.00866U(t-t_2)\left\{e^{-0.36\times10^6(t-t_2)} - e^{-3.31\times10^6(t-t_2)}\right\}$$
$$+ V_{eq}U(t-t_1)[-0.000036e^{-0.36\times10^6(t-t_1)} - 0.000989e^{-3.31\times10^5(t-t_1)} + 0.001025e^{-2.56\times10^6(t-t_1)}]. \tag{20}$$

The dominating term in (20) is

$$[0.00375V_{eq} - 0.00866]U(t-t_1)\left\{e^{-0.36\times10^6(t-t_1)} - e^{-3.31\times10^6(t-t_1)}\right\}. \tag{21}$$

If V_{eq} is large enough, this term is positive; otherwise, the term is negative. In order to match the corresponding waveform in Fig. 7(b), it is necessary for V_{eq} to have a magnitude great enough to overcome the negative unblanking pulse and give a positive magnitude corresponding to $+48$ v. If this is to be the case, then

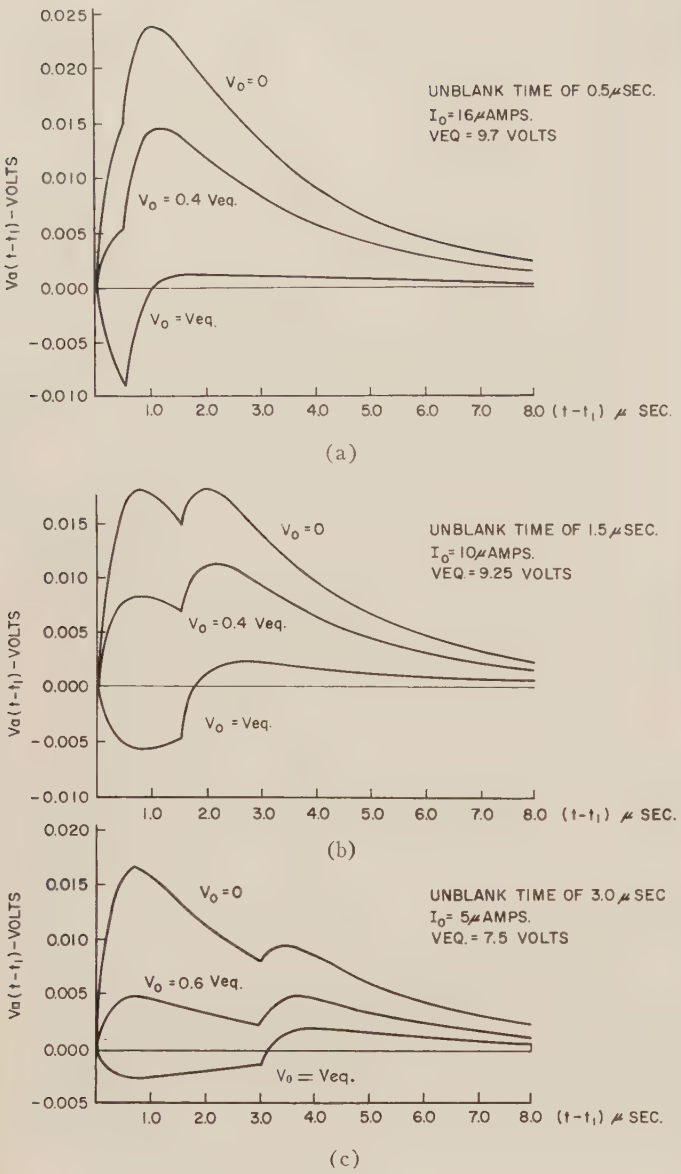


Fig. 6—Theoretical dot-reading-dot waveforms for different operating conditions.

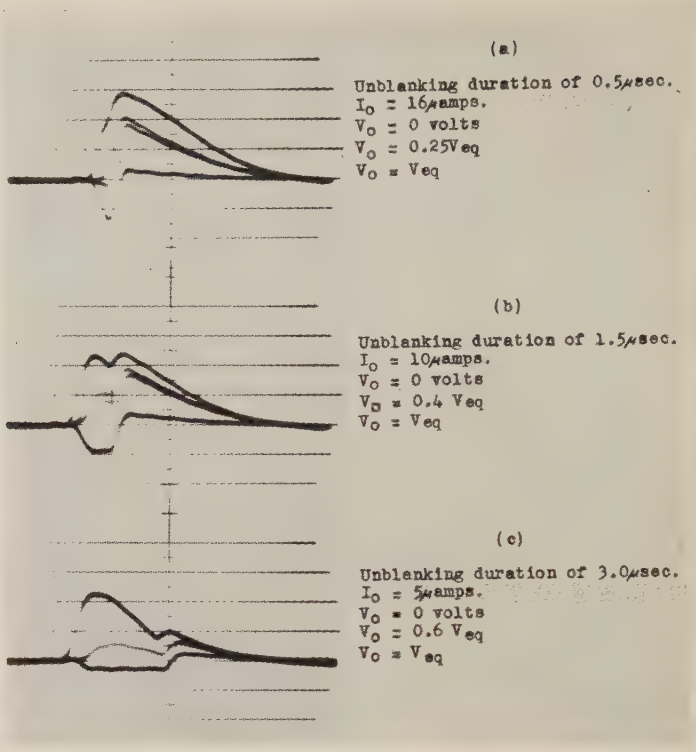


Fig. 7—Experimental dot-reading-a-dot waveforms which correspond to the same operating conditions as Fig. 6. Sweep time = 1 μsec/cm. Vertical deflection = 20 v/cm.

$$\frac{-0.00866K}{-16} = \frac{x}{+48}, \qquad x = 0.02598K \tag{22}$$

where K is a constant of proportionality which can be used as a first approximation for relating plotted quantities with actual waveforms; x is the magnitude needed in (21) to make the plotted curve correspond to 48 v. So, for the plotted curve to correspond to +48 v, V_{eq} must be

$$0.00375K\,V_{eq} - 0.00866K = 0.02598K \tag{23}$$

$$V_{eq} = \frac{0.03464}{0.00375} = 9.25\text{v}. \tag{24}$$

It is interesting to note that this value of $V_{eq} = 9.25$ v compares quite well with values given by Kates.[2] See Fig. 8. The shape of this curve is very much like that of Fig. 3 in which the spot diameter is plotted against the peak beam current I_0. By combining the information contained in Figs. 3 and 8, a plot can be made of V_{eq} vs the spot diameter as shown in Fig. 9. It is seen that V_{eq} increases linearly with the spot diameter within the range of 0.030 inch to 0.060 inch of spot diameter. This gives a convenient method of estimating the spot potential by simply measuring the spot diameter.

The dot-reading-a-dot experiments made in this section show that the equation for $V_a(t-t_1)$ can be used to determine the actual output waveforms. By using the information shown graphically in Figs. 3 and 8, it should be possible to predict actual output signals for different operating conditions.

III. Dot-Circle Experiments

Dot-Read Waveforms

Fig. 10 shows what the waveforms look like when operating parameters are chosen to accentuate the difference between dot-reading-a-circle signals and dot-reading-a-dot signals. The family of all four dot-circle output signals with no refill present at the time of bombardment is seen in Fig. 10(c). From top to bottom in Fig. 10(c) the waveforms are 1) circle reading a dot,

[2] J. Kates, "Space Charge Effects in Cathode-Ray Storage Tubes," University of Toronto, Ont., Canada, Ph.D. Dissertation in physics; 1951.

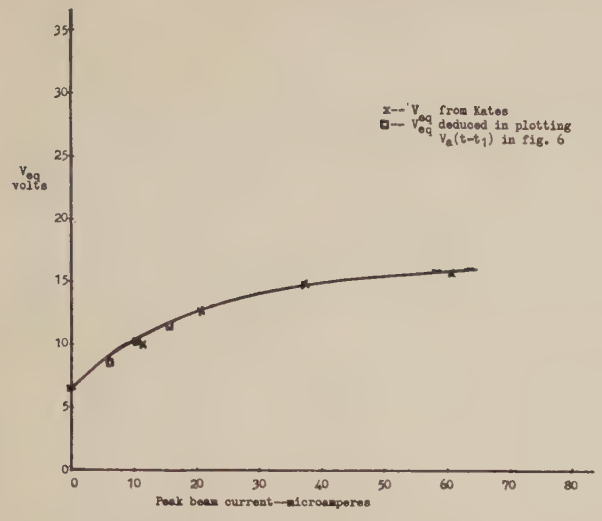


Fig. 8—Variation of the equilibrium spot potential V_{eq} vs peak beam current.

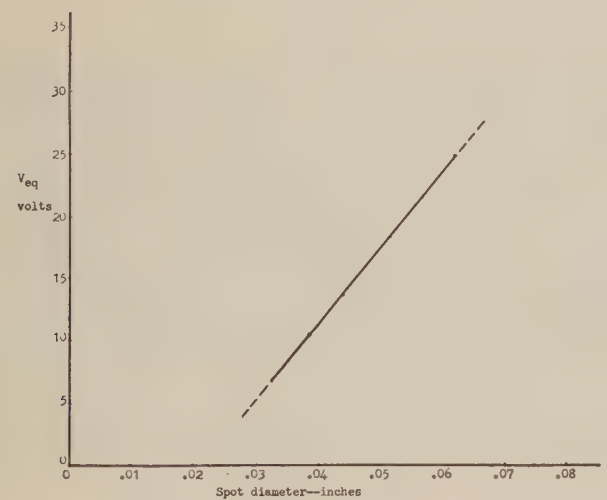


Fig. 9—Variation of equilibrium spot potential vs spot diameter.

2) dot reading a dot, 3) circle reading a circle, and 4) dot reading a circle. In this case the amplitude difference between circle-read signals is greater than for dot-read signals; however, in Fig. 10(b) the difference between circle-read signals has nearly disappeared with only 10 per cent refill present at the time of bombardment. (See Fig. 2 for the percentage change in charge for $n=31$ and a separation of 0.060 inch. Fig. 2 does not represent exactly the same operating conditions as Fig. 10, but it is close enough for a good first approximation in estimating the percentage of refill.) The dot-read waveforms of Fig. 10(b), on the other hand, are still quite distinguishable. Fig. 10(a) shows about 35 to 40 per cent refill present at the time of bombardment. The circle-read signals are identical. For the same percentage of refill, the dot-read curves still show a difference. If the dot-read signals are sampled just before unblanking ends, the distinction between a stored "0" and a stored "1" can always be detected. In Fig. 10(a) the dot-reading-a-circle signal is always more negative than −9

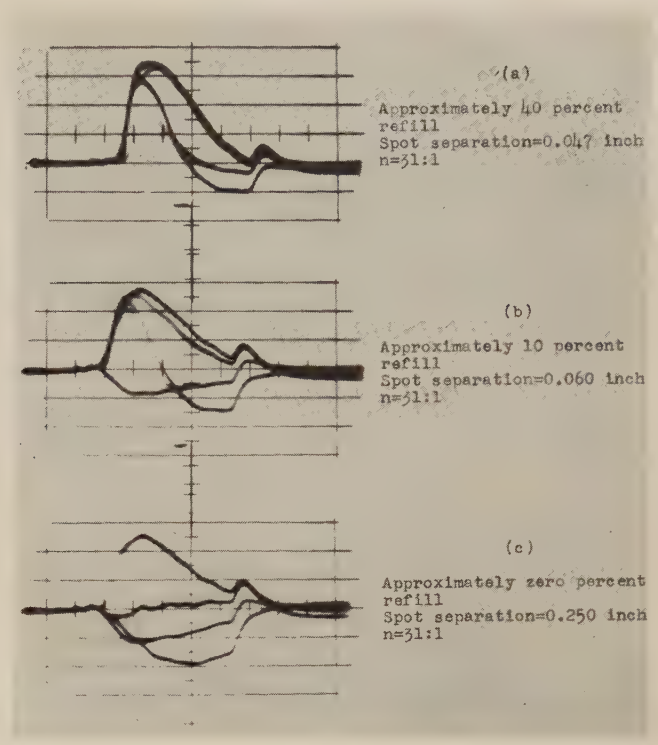


Fig. 10—Dot-circle waveforms with operating parameters chosen to accentuate the difference between dot-read output signals. Input resistance to amplifier = 28,000 ohms, circle frequency = 2 mc, unblanking duration = 4.5 μsec, circle diameter = 0.058 inch, peak beam current = 6.7 μamp, dot diameter = 0.039 inch, horizontal sweep time = 1 μsec/cm, and vertical deflection = 10 v/cm.

v, whereas the dot-reading-a-dot signal is never more negative than −5 v.

Theoretical Dot-Read Waveforms

An expression is developed now which gives the dot-read output waveforms. The same equivalent circuit is used as in Section II and a term is added to the driving current i to account for the discharging effects of a circle read by a dot. The driving current becomes

$$i = -I_0[U(t-t_1) - U(t-t_2)] + M\exp -\frac{t-t_1}{R_2(C_1+C_3)} - L(t-t_1)e^{-r(t-t_1)} \qquad (25)$$

where L and r are constants to be determined from experiment. The reason the discharge term is taken to be

$$-L(t-t_1)e^{-r(t-t_1)}$$

is that by observing the output waveforms for a dot reading a circle, it was seen that the term involving the discharge of the outer ring of the circle should have a large time constant and that as time increased, the magnitude of the waveform should remain nearly constant. This would be possible, if, as the exponential caused a decay of the waveform towards zero, a term increasing with time could be included to help hold the magnitude fixed.

If the two simultaneous equations given in (14) are written with the discharging term $-L(t-t_1)e^{-r(t-t_1)}$ added to the driving current, then $V_a(t-t_1)$ becomes

$$V_a(t-t_1) = \frac{C_1(V_{eq}-V_0)}{R_4P(s_1-s_2)}\,U(t-t_1)\{e^{s_1(t-t_1)}-e^{s_2(t-t_1)}\}$$

$$-\frac{C_1I_0}{P(s_1-s_2)}\left[U(t-t_1)\{e^{s_1(t-t_1)}-e^{s_2(t-t_1)}\}-U(t-t_2)\{e^{s_1(t-t_2)}-e^{s_2(t-t_2)}\}\right]$$

$$+\frac{C_1M}{P}\,U(t-t_1)\left[\frac{s_1e^{s_1(t-t_1)}}{(s_1-s_2)\left(s_1+\frac{1}{R_2(C_1+C_3)}\right)}+\frac{s_2e^{s_2(t-t_1)}}{(s_2-s_1)\left(s_2+\frac{1}{R_2(C_1+C_3)}\right)}\right.$$

$$\left.-\frac{\frac{1}{R_2(C_1+C_3)}\exp-\frac{t-t_1}{R_2(C_1+C_3)}}{\left(s_1+\frac{1}{R_2(C_1+C_3)}\right)\left(s_2+\frac{1}{R_2(C_1+C_3)}\right)}\right]$$

$$-\frac{C_1L}{P}\,U(t-t_1)\left[\frac{s_1e^{s_1(t-t_1)}}{(s_1-s_2)(s_1+r)^2}+\frac{s_2e^{s_2(t-t_1)}}{(s_2-s_1)(s_2+r)^2}+\frac{(r^2+s_1s_2)e^{-r(t-t_1)}}{(s_1+r)^2(s_2+r)^2}-\frac{r(t-t_1)e^{-r(t-t_1)}}{(s_1+r)(s_2+r)}\right] \quad (26)$$

After trying several different values for r, it was ascertained that $r=0.01\times10^6$ second^{-1} gave about the best match with actual waveforms when the following values were used in plotting the curves of Fig. 11:

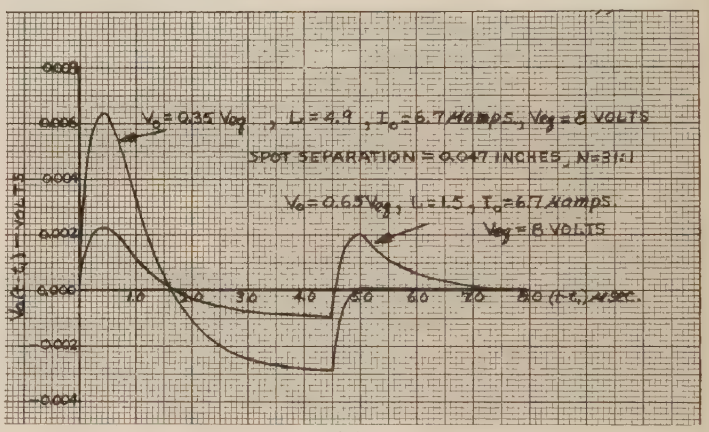
$R_1 = 10^6$ ohms, $C_1 = 0.1$ $\mu\mu$f,
$R_2 = 3\times10^5$ ohms, $C_2 = 30$ $\mu\mu$f,
$R_3 = 28\times10^3$ ohms. $C_3 = 1.2$ $\mu\mu$f.

The expressions for s_1, s_2, P, R_4, and M are the same as those given in Section II. The values of V_{eq}, V_0 are determined by the operating parameters. L was chosen to make the theoretical curves match the actual waveforms as closely as possible. V_{eq} is dependent upon I_0, the peak beam current. $I_0=6.7$ μamp. The dot diameter for this current was 0.0385 inch. From Fig. 9 it can be seen that V_{eq} has the value of 8 v.

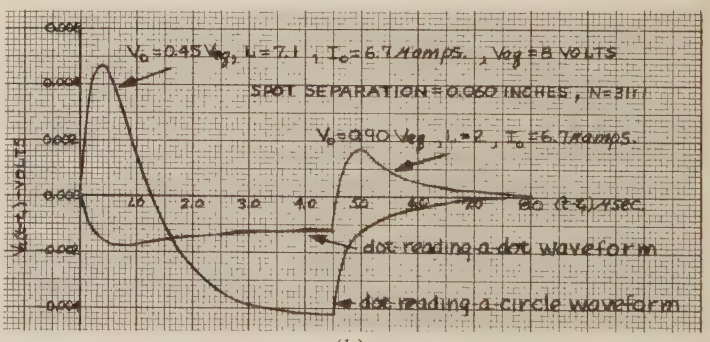
The value of L depends upon the amount of charge present in the positive ring surrounding the dot at the time of bombardment. In the case of a dot reading a circle having zero refill, the value of L which matched the output waveforms was $L=7.9$ amp per second.

In plotting the curves of Fig. 11, the contribution of the two terms containing $e^{-r(t-t_1)}$ were terminated as soon as the response of the equivalent circuit reached its most positive magnitude after the primary beam was turned off. This occurred at $(t-t_1)=5$ μsec. Whatever magnitude of $V_a(t-t_1)$ existed at that time was allowed to decay towards zero with the time constant of the amplifier input, namely, $R_3C_2=(0.028\times10^6)(30\times10^{-12})$ seconds.

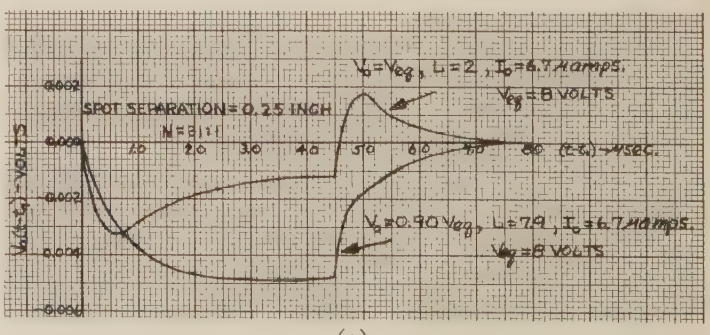
By examining Fig. 11 closely, one can get a good idea of the charge patterns at the deflected spot at the time of bombardment. In Fig. 11(c) the dot-reading-a-circle signal came first. The value assumed for L was 7.9 amp per second. After the primary beam bombarded the spot for 4.5 μsec, L was reduced to 2 amp per second. This means that the dot discharged approximately three



(a)



(b)



(c)

Fig. 11—Theoretical dot-read waveforms.

ourths of the outer area of the circle during the reading bombardment.

The values chosen for V_0 in plotting the dot-reading-a-dot signals of Fig. 11 were obtained from Fig. 2. For example, with $n=31$ and with a spot separation of 0.250 inch as is the case in Fig. 11(c), the corresponding percentage change of the output waveform Y is approximately zero. This means that the spot was still charged to its equilibrium potential at the time of examination, so $V_0 = V_{eq}$. In the case of a dot reading a dot as in Fig. 11(b) with a spot separation of 0.060 inch and $n=31$ and Y of Fig. 2 having the value of 10 per cent that is, refill had reduced the positive equilibrium potential V_{eq} by 10 per cent, $V_0 = 0.90\ V_{eq}$. In Fig. 11(a) where the spot separation was 0.047 inch, the corresponding change of Y, Fig. 2, is 35 per cent, meaning that V_{eq} had been reduced by 35 per cent, thus $V_0 = 0.65\ V_{eq}$.

The main difference between the theoretical and actual curves occurs in the time taken for the positive pulses to cross the base line. In the actual case, Fig. 10, approximately 2.5 μsec elapse before the crossover occurs, whereas only 1.5 μsec elapse in Fig. 11. Otherwise, the theoretical curves compare quite favorably with the actual waveforms.

The values chosen for V_0 in the case of the dot-reading-a-circle signals of Fig. 11 did not correspond to the percentage changes of Y in Fig. 2. The values of V_0 in this case are less. To see why this is true, consider the situation as a circle is being written. The area immediately under bombardment of the beam is charging whereas the area just outside the traveling beam is being discharged. When the beam is turned off, part of the dot-read area, indicated by the shaded region of Fig. 12, remains partially discharged. Thus, during reading when the dot hits the center of the circle there is considerably more positive charging of the spot than would have resulted from refill alone. The additional destruction of the dot area within the circle while writing the circle causes the early portion of the dot-reading-a-circle output waveforms to be more positive.

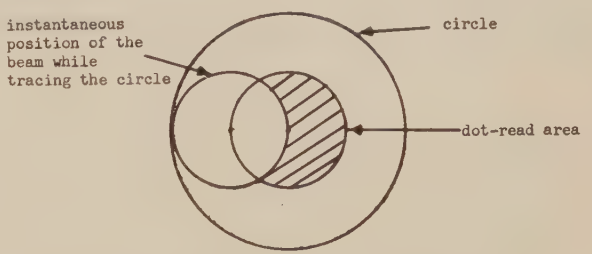


Fig. 12—Writing a circle with a focused dot.

The value chosen for L determines how negative the output waveforms will go after the initial positive charging effects have dissipated themselves. L is chosen in each case to give a reasonably good match with the actual output waveforms of Fig. 10. The maximum L was 7.9 amp per second as in Fig. 10 (c) while the minimum L was 1.5 amp per second as shown in Fig. 10(a).

Computing and Error Matrices in Linear Differential Analyzers*

AMOS NATHAN†

Summary—**Matrix formulation permits the compact analysis of a very general computing scheme based on operational amplifiers. The computer solves an equation in which a computing matrix and an error matrix can be distinguished. Programming a differential equation consists of writing it in an appropriate matrix form. The computing setup is in immediate mutual correspondence with the computing matrix. The error matrix can be written down by inspection.**

Introduction

HONNELL and Horn, in some recent papers,[1,2] use matrix methods to analyze the most general setup of linear analog differential analyzers consisting of operational amplifiers, passive input and feedback admittances, and their interconnections. The objects and results are interesting; the network analysis part of their papers is, however, extraordinarily circuitous and an independent derivation will be in order.

The present paper considers ordinary operational amplifiers as basic elements whereas Honnell and Horn choose units with both positive and negative outputs.

The Computing Network

Fig. 1 represents the αth basic operational unit. It consists of $n+m$ terminals $1, 2, \cdots, (n+m)$; $n+m$ linear bilateral admittances $Y_{\alpha\beta}$, $\alpha=1, 2, \cdots, n$, $\beta=1, 2, \cdots, (n+m)$, between terminal β and node (or line) l_α; and a linear operational amplifier flowing from l_α into α, of gain A_α, infinite input impedance and zero output impedance, the latter being a well-justified approximation. Let $\overline{A}_\alpha(p)$ be the transmittance of the amplifier, so that $\overline{A}_\alpha(0)=A$. Terminal α is the output terminal of this unit; all others are input terminals.

Let n basic operational units be interconnected as shown in Fig. 2, which illustrates the case $n=4$, $m=2$.

Considering first $m=0$, we have here the most general permissible interconnection of n operational amplifiers and n nodes through admittances $Y_{\alpha\beta}$, for each input connects through some admittance with each node. Amplifier outputs must not be shorted but must also connect with a node through some admittance. For $m\neq 0$, terminals $n+1, \cdots, n+m$ will be used to supply the driving inputs. Note that additional setups could be constructed if more than n nodes and all permissible interconnections were provided for n amplifiers. Our narrower point of view leaves, however, very wide latitude.

* Manuscript received by the PGEC, May 30, 1957.

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[1] P. M. Honnell and R. E. Horn, "Analogue computer synthesis and error matrices," *Trans. AIEE (Commun. and Electronics)*, no. 23, pp. 26–32; March, 1956.

[2] P. M. Honnell and R. E. Horn, "Matrices in analogue mathematical machines," *J. Franklin Inst.*, vol. 260, pp. 193–207; September, 1955.

The Network Equations

Let v_β, $\beta=1, 2, \cdots, n+m$, be the voltage of terminal β, and let v_{l_α}, $\alpha=1, 2, \cdots, n$ be the voltage of line l_α. The current equation (Kirchhoff I) for line l_α then reads

$$\sum_{\beta=1}^{n+m} Y_{\alpha\beta}(v_\beta - v_{l_\alpha}) = 0, \qquad \alpha = 1, 2, \cdots, n. \tag{1}$$

The operational amplifiers impose the constraints

$$v_{l_\alpha}\overline{A}_\alpha = v_\alpha, \qquad \alpha = 1, 2, \cdots, n. \tag{2}$$

Using (2) to eliminate v_{l_α} from (1) we have finally

$$\sum_{\beta=1}^{n+m} Y_{\alpha\beta}v_\beta = \sum_{\beta=1}^{n+m} \frac{Y_{\alpha\beta}}{\overline{A}_\alpha} v_\alpha, \qquad \alpha = 1, 2, \cdots, n. \tag{3}$$

$v_{n+1}, \cdots, v_{n+m}$ are given voltage sources and (3) thus solves the problem.

Let us present the solution in the more majestic matrix form. For (3) write

$$\sum_{\beta=1}^{n+m} Y_{\alpha\beta}v_\beta = \sum_{\gamma=1}^{n} \left[\sum_{\beta=1}^{n+m} \frac{Y_{\alpha\beta}}{\overline{A}_\gamma} \delta_{\alpha\gamma} \right] v_\gamma, \alpha = 1, 2, \cdots, n, \tag{3a}$$

which is the same as

$$\begin{Vmatrix} Y_{11} & Y_{12} \cdots Y_{1,n+m} \\ Y_{21} & Y_{22} \cdots Y_{2,n+m} \\ \cdot & \\ \cdot & \\ Y_{n1} & Y_{n2} \cdots Y_{n,n+m} \end{Vmatrix} \cdot \begin{Vmatrix} v_1 \\ v_2 \\ \cdot \\ \cdot \\ v_n \\ v_{n+1} \\ \cdot \\ \cdot \\ v_{n+m} \end{Vmatrix}$$

$$= \begin{Vmatrix} \sum_{\beta=1}^{n+m} \frac{Y_{1\beta}}{\overline{A}_1} & & & \\ & \sum_{\beta=1}^{n+m} \frac{Y_{2\beta}}{\overline{A}_2} & & \\ & & \cdot & \\ & & & \sum_{\beta=1}^{n+m} \frac{Y_{n\beta}}{\overline{A}_n} \end{Vmatrix} \cdot \begin{Vmatrix} v_1 \\ v_2 \\ \cdot \\ \cdot \\ v_n \end{Vmatrix}; \tag{4}$$

or, for short,

$$y \cdot v = y_{\epsilon A} \cdot v'. \tag{4a}$$

y is appropriately called the computing matrix; $y_{\epsilon A}$ is the error matrix; v is the complete voltage vector; and v', consisting of the first n components of v, is the output voltage vector. Note the close correspondence of y and v

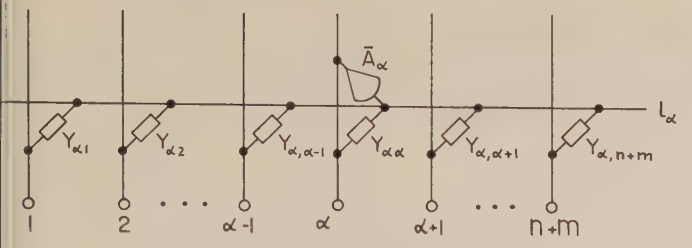

Fig. 1—The αth basic operational unit.

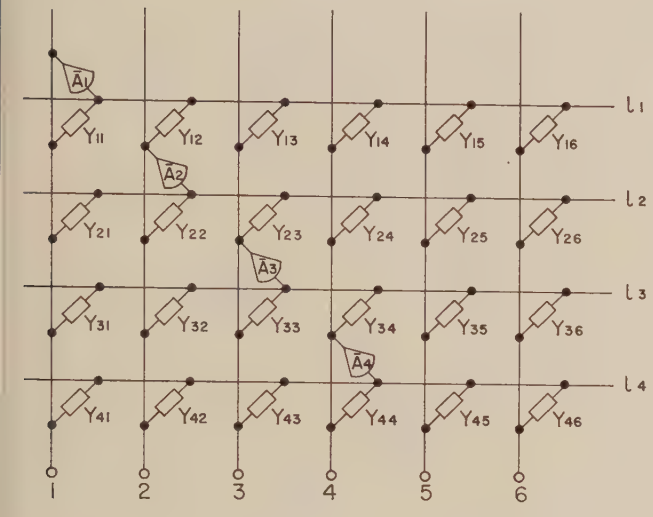

Fig. 2—The general computing matrix.

with Fig. 2, which makes the actual drawing of the figure quite superfluous.

The error matrix $y_{\epsilon A}$ due to the finite gains of the amplifiers is diagonal; this matrix usually yields the major contribution to dynamic errors. Other errors may lead to error matrices which are not necessarily diagonal. The error matrices are of importance in the consideration of accuracy and stability.

Analog Solution of Differential Equations

It is the task of the programmer to match the ideal network equation

$$yv = 0 \tag{5}$$

with the given differential equation; the computer then solves (4) instead. For this purpose the problem is first written in matrix form. For general considerations relating to this problem the reader is referred to Honnell and Horn.[2] We shall be content here with some general remarks and an example.

All entries in y must be positive forms in the Laplacian operator p. Moreover, for familiar reasons, let us limit ourselves to the use of conductances and capacitances as passive elements. For the sake of illustration let us further demand that capacitances appear as direct feedback elements only, which means that entries of the form $(G_{\alpha\alpha}+pC_\alpha)$ can appear on the principal diagonal of y; all other entries must be conductances, $y_{\alpha\beta}=G_{\alpha\beta}$, $\alpha\neq\beta$.

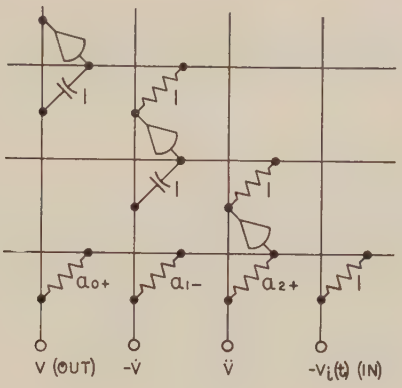

Fig. 3—Matrix for $a_{2+}\ddot{v}-a_{1-}\dot{v}+a_{0+}v=v_i(t)$.

Consider the differential equation

$$a_n\frac{d^nv}{dt^n}+a_{n-1}\frac{d^{n-1}v}{dt^{n-1}}+\cdots+a_1\frac{dv}{dt}+a_0v=v_i(t), \tag{6}$$

which becomes in Laplace transform notation

$$a_np^n\bar{v}+a_{n-1}p^{n-1}\bar{v}+\cdots+a_1p\bar{v}+a_0\bar{v}=\bar{v}_i(p). \tag{6a}$$

One way of putting (6a) into the required matrix form (5) is

$$\begin{Vmatrix} 1 & 1 & \cdot & \cdot & \cdot & \cdot & & & \\ \cdot & p & 1 & \cdot & \cdot & \cdot & & & \\ \cdot & \cdot & 1 & 1 & \cdot & \cdot & & & \\ \cdot & \cdot & \cdot & p & 1 & \cdot & & & \\ \cdot & & & & & \cdot & & & \\ & & & & & & 1 & 1 & \cdot \\ a_{0+} & a_{0-} & a_{1+} & a_{1-} & \cdots & & a_{n+} & a_{n-} & 1 \end{Vmatrix} \cdot \begin{Vmatrix} \bar{v} \\ -\bar{v} \\ p\bar{v} \\ -p\bar{v} \\ \cdot \\ \cdot \\ p^n\bar{v} \\ -p^n\bar{v} \\ -\bar{v}_i \end{Vmatrix} = 0 \tag{7}$$

where $a_\alpha=a_{\alpha+}$, $a_{\alpha-}=0$ if $a_\alpha>0$ and $a_\alpha=a_{\alpha-}$, $a_{\alpha+}=0$ if $a_\alpha<0$. Not all entries will, in general, be present. For example

$$a_{2+}p^2\bar{v}-a_{1-}p\bar{v}+a_{0+}\bar{v}=\bar{v}_i \tag{8}$$

reduces (7) to

$$\begin{Vmatrix} p & 1 & 0 & 0 \\ 0 & p & 1 & 0 \\ a_{0+} & a_{1-} & a_{2+} & 1 \end{Vmatrix} \cdot \begin{Vmatrix} \bar{v} \\ -p\bar{v} \\ p^2\bar{v} \\ -\bar{v}_i \end{Vmatrix} = 0, \tag{8a}$$

which is realized in Fig. 3. Initial conditions must be taken care of in the usual manner; alternatively (6a) could be written so as to include initial conditions and then reshaped into (5). The error matrices can be written down by inspection.

Scanners for Ferroelectric Memory Capacitors*

C. F. PULVARI† AND G. E. McDUFFIE, JR.†

Summary—Many references are available on the properties and characteristics of ferroelectric materials and their memory application.[1–3] The purpose of this paper is to present several scanning systems by which binary information can be stored and recalled from ferroelectric capacitor configurations. The circuitry to be described here was originally designed for testing of ferroelectric elements and employs an ordered or nonrandom scanning pattern. Most of the circuitry presented is, however, adaptable to random access application.

Introduction

FIG. 1 shows the hysteresis plot of charge vs applied voltage for a storage cell with nearly rectangular characteristics. For purposes of this paper the $+Q_r$ state is defined as the binary zero ("0") state of the storage element and the $-Q_r$ state is defined as the binary one ("1") state. The rest or "set" state of an array is defined as the "0" state, *i.e.*, an array is initially set to store "0"s in all storage cells. Words are written into an array by switching those cells corresponding to the "1"s of a word to the $-P_r$ state of polarization.

Either destructive or nondestructive readout may be used to recall stored information.[4] The systems to be described are intended for destructive readout although they may be modified for nondestructive readout. In destructive readout, each element of the array is sensed with positive pulses. When a cell in the "0" state is sensed, no switching of polarization results; when an element in the "1" state is sensed, the charge of the ferroelectric is switched from the $-Q_r$ to the $+Q_r$ state. Various methods for detecting the switching of polarization have been described and will not be covered in this paper.[4]

Fig. 2, however, shows a single destructive write-read circuit and the waveforms resulting from "0" and "1" signals.

Requirements of a Ferroelectric Scanner

In order to write and read information into and out of a multicondenser array of storage cells, it was necessary to develop switching circuitry which met the following requirements:

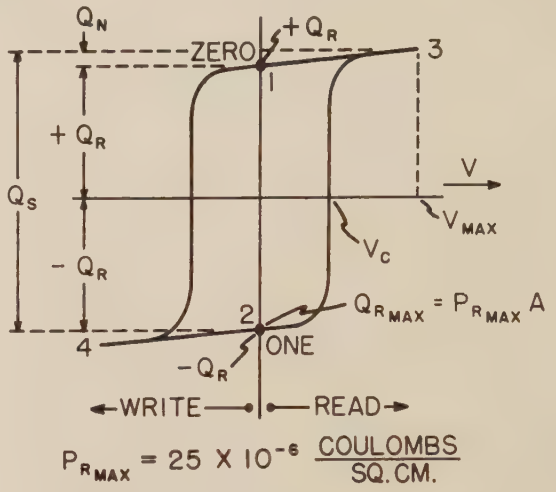

Fig. 1—Hysteresis loop of a ferroelectric storage cell.

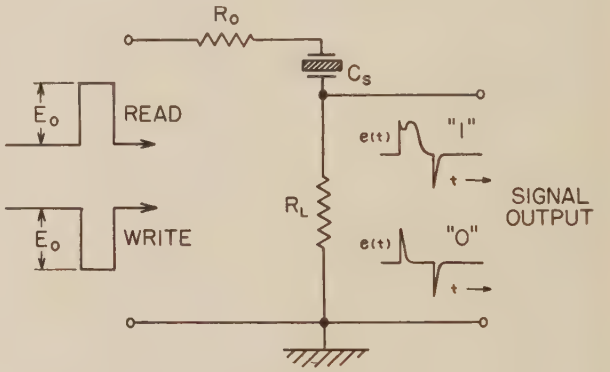

Fig. 2—Basic storage circuit.

1) Provide pulses of both positive and negative polarity.
2) Provide gating action for both positive and negative pulses.
3) Provide an impedance match between the ferroelectric storage cells and the pulse source. As little as 1 to 5×10^{-6} watt-seconds of energy are required to switch a single cell. However, the power needed is a function of the type of array and the desired speed of operation.
4) Provide a convenient method for obtaining readout signals.
5) Ordered or random access should be possible.
6) Physical size of circuitry should be compatible with the small size of the ferroelectric array.

In general, a scanner consists of a device for generating pulses of either polarity in ordered or random sequence and a switching system capable of selecting the desired storage cells from an array. Several systems for performing these operations on several different arrays have been constructed and tested and are described here.

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† Dept. of Elec. Eng., Catholic University of America, Washington, D. C.

[1] C. F. Pulvari, "Ferroelectrics and their memory applications," IRE TRANS. ON COMPONENT PARTS, vol. CP-3, pp. 3–11; March, 1956.

[2] J. R. Anderson, "Ferroelectric materials as storage elements for digital computers and switching systems," *Elec. Eng.*, vol. 71, pp. 916–922; November, 1952.

[3] G. Shirane, F. Jona, and R. Pepinsky, "Some aspects of ferroelectricity," PROC. IRE, vol. 43, pp. 1738–1793; December, 1955.

[4] C. F. Pulvari and G. E. McDuffie, Jr., "Signals from switched ferroelectric storage condensers," *Trans. AIEE (Commun. and Electronics)*, vol. 28, pp. 681–685; January, 1957.

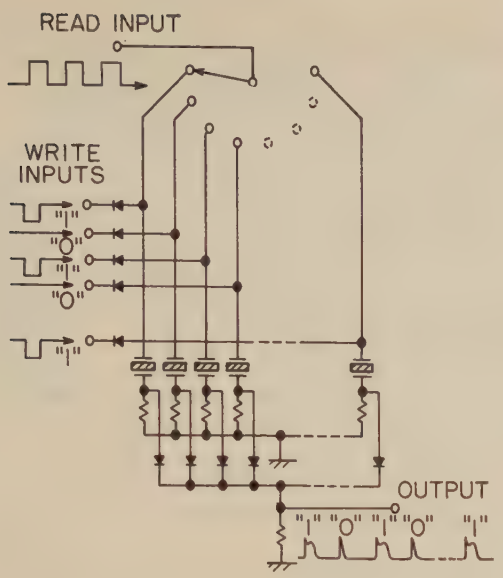


Fig. 3—Parallel-series linear scanner.

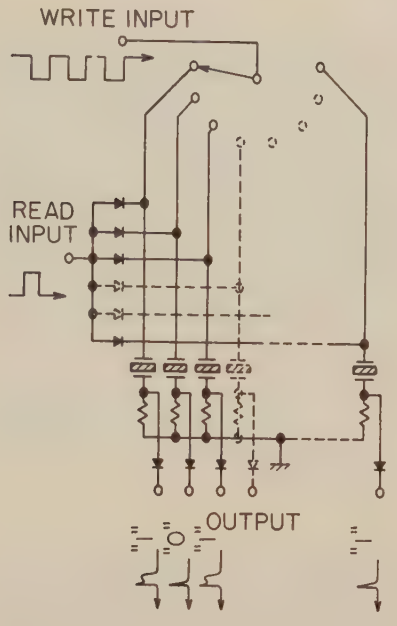


Fig. 4—Series-parallel linear scanner.

Linear Scanners

Ferroelectric storage cells may be arranged in a linear type array, *i.e.*, in a single line. Input and output can be obtained in the following modes: 1) parallel input and output, 2) parallel input, serial output, 3) serial input and output, 4) serial input, parallel output. As an illustration, Fig. 3 shows a parallel-series type of arrangement. The information to be stored is simultaneously written on the n parallel leads (shown at the left of Fig. 3) by the application of negative pulses to the leads corresponding to the binary "1"s of the word. The information is read out of the memory by the application of positive read pulses to the input terminal. After each read pulse the switch is advanced to the next position and another read pulse is applied to the read input terminal. Thus, the information is simultaneously written into the memory on parallel leads and read out in sequence on a single lead.

The "dual" of this system is a series-parallel arrangement and is shown in Fig. 4. In this mode, the information is written into the memory by the application of negative pulses, in sequence, to the input lead and read out simultaneously on the parallel leads.

Many counter systems are adaptable as linear scanners for either parallel-series or series-parallel arrangements of ferroelectric storage cells. The beam switching tube, developed by Burroughs, Inc., is particularly suited to this form of operation. The beam switching tube is, in essence, a decade counter capable of operation at speeds from dc to several megacycles and can furnish sufficient pulse power to switch ferroelectric storage capacitors at relatively high speeds. Several tubes can be serially connected to scan a relatively long line of storage capacitors.

Linear scanning of ferroelectric storage cells is restricted to relatively small memories because of the large amount of circuitry per bit of information. However, the selection of ferroelectric cells for this type of array is far less restrictive than that required for matrix-type configurations. The amplitude of the applied pulses is not critical and, for a given crystal thickness, depends upon the desired switching time.

Square-Matrix Scanning

One means of reducing the amount of electronic circuitry per bit of information is to arrange the storage capacitors in the form of a matrix.[2,5] Fig. 5 shows the arrangement of the storage cells in a matrix array and the approximate equivalent circuit. Two types of matrix scanning will be discussed: 1) "simple" matrix scanning in which the ratio of voltage across the selected cross-point is 2:1 and 2) pulse bias scanning in which the above ratio is k:1. The highest voltage across an unselected cross point occurs across the elements connected to the selected rows and columns; the $(n-1)C$ capacitors in the equivalent circuit of Fig. 5 represent these storage cells.

Simple scanning, as used here, is the application of pulses of amplitude $\pm V/2$ to the row leads and $\mp V/2$ to the column leads of the ferroelectric storage matrix as shown in Fig. 5, where these pulses are in time coincidence. From the equivalent circuit of the matrix it can be seen that this type of operation introduces pulses of amplitude $\pm V$ on the selected ferroelectric storage capacitor and pulses of amplitude $\pm V/2$ on the capacitors connected to the selected row and column.

Pulse bias scanning is a method by which the voltage across the unselected storage cells, connected to selected row and column leads, is reduced to a value V/k which is less than $V/2$. In bias scanning, pulses of amplitude $\pm V/2$ and $\mp V/2$ are applied to the rows and columns and, in coincidence with these main switching pulses,

[5] C. F. Pulvari, "Memory matrix using ferroelectric condensers as bistable elements," *Assn. for Computing Machinery J.*, vol. 2, pp. 169–185; July, 1955.

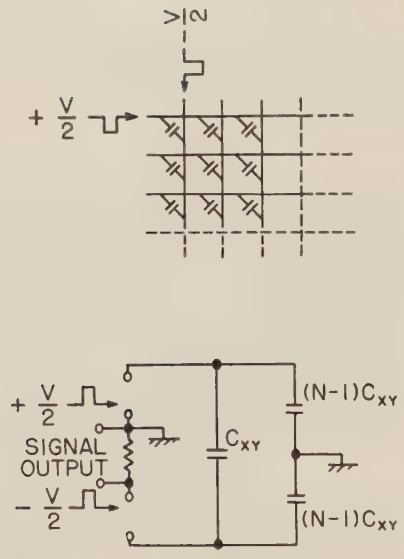


Fig. 5—Equivalent circuit of simply scanned square matrix.

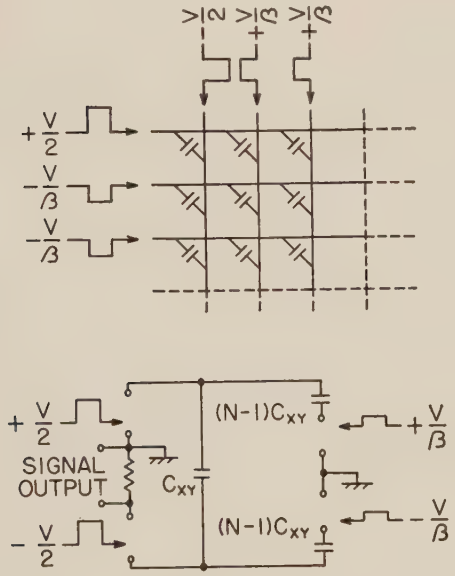


Fig. 6—Equivalent circuit of pulse-bias scanned matrix.

pulses of amplitude $\mp V/\beta$ and $\pm V/\beta$ are applied to the unselected row leads and column leads, as shown in Fig. 6. Pulses of amplitude V/β subtract from the $V/2$ pulses normally present on the unselected elements reducing the so-called noise voltage to V/k, thus providing a selected-to-nonselected ratio of V to V/k. The advantage of such a system is that it reduces the amplitude of the disturbing voltage on the unselected elements, allowing construction of larger matrices with a given type of storage cell than is possible with a V-to-$V/2$ ratio.

The amplitude of the pulse bias voltage V/β cannot be increased indefinitely as can be seen by examining the indicated storage cells on cross points connected to the unselected rows and columns. On these cross points a voltage of amplitude $2V/\beta$ now occurs, whereas in simple scanning this voltage is negligible. The maximum

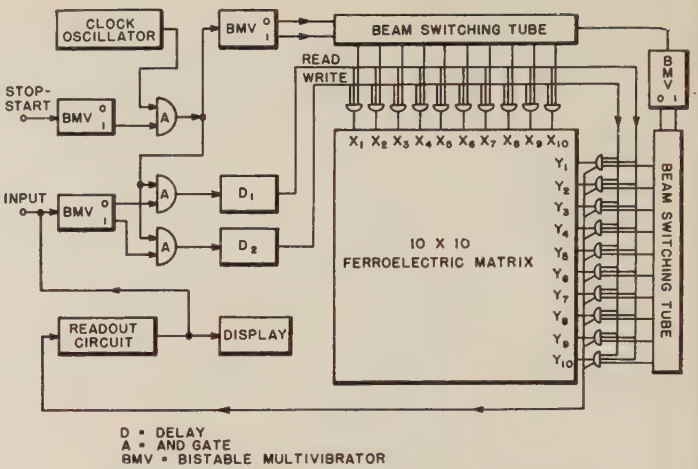


Fig. 7—Block diagram of 10×10 matrix scanner.

allowable value of V/β occurs when the magnitude of the voltage across the unselected cross points, connected to the selected columns and rows, is equal in magnitude to the voltage across the remaining unselected cross points, *i.e.*, when

$$\frac{V}{k} = \frac{V}{2} - \frac{V}{\beta} = \frac{2V}{\beta} \tag{1}$$

which gives $\beta = 6$ and $k = 3$. Thus, the best ratio possible for pulse bias scanning is V to $V/3$.

A 10×10 Scanner

Fig. 7 shows a simplified block diagram of a 10×10 matrix scanner designed to be used with ferroelectric storage capacitors. The device may be operated as either a simple scanner or a pulse biasing scanner. Basically, the device consists of two pulse sources with negative outputs of amplitude $V/2$ (a write pulse generator and a read pulse generator) and means for distributing the outputs of these generators to the storage cells. The outputs from the two pulse sources are connected to ten column gates and to ten row gates. The column gates are opened sequentially by the column counter driven at the clock repetition rate; the row gates are opened sequentially by the row counter driven sequentially at one tenth the clock repetition rate. Thus, access is provided to each element of the matrix in the normal 11, 12, · · · , 21, 22, · · · , sequence.

The $-V/2$ pulses from the read generator passing through the column gates are inverted giving rise to $+V/2$ read pulses on column leads; $-V/2$ pulses from the write generator are not inverted when passed through the column gates and produce $-V/2$ write pulses on the column leads. The opposite sequence is followed in the row gates resulting in $-V/2$ read pulses and $+V/2$ write pulses on the row leads. In this manner, each selected cross point in simple scanning is driven by a $+V$ read pulse and a $-V$ write pulse, considering the upper left-hand ends of the storage cells to be the reference points.

Row and column counters employ Burroughs MO-10

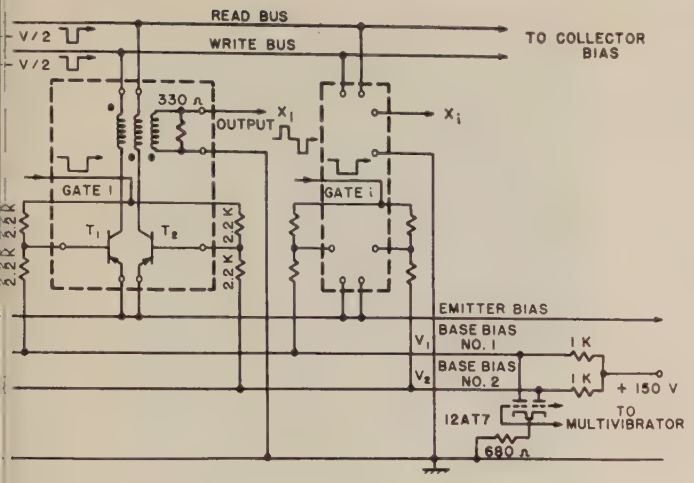


Fig. 8—Bidirectional transistor gate.

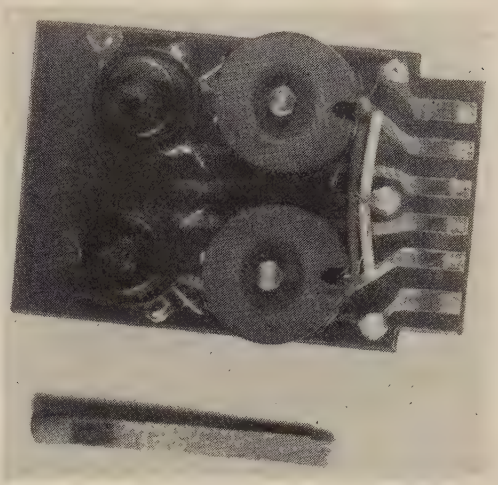


Fig. 9—Transistor gate assembly.

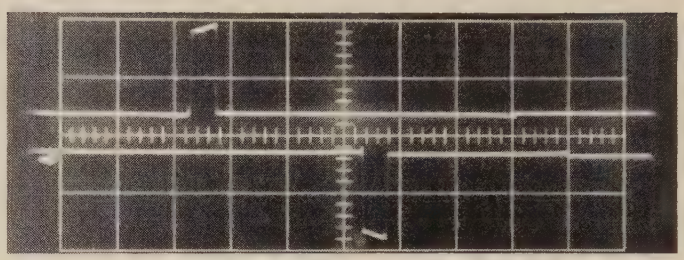


Fig. 10—Transistor gate output waveform (5 μsec and 10 volts per large division).

beam switching tubes as decimal counters.[6] The control gates are driven by negative pulses taken from the targets of the switching tubes. Both beam switching tubes are driven by bistable multivibrators. The write and read generators are identical pulse generators employing 6AS7 output tubes and capable of delivering 40-volt pulses, 1 to 10 μsec in duration, at 100 ohms and at repetition rates up to 200 kc.

The column and row gates are bidirectional "and" gates employing junction transistors as common emitter switches.[7] A simplified circuit diagram of the gate is shown in Fig. 8. The write and read buses, emitter bias, and write and read bias are common to all gates. Read bias V_1 and write bias V_2 are controlled by a bistable multivibrator. When simple scanning is used, operation is as follows: if a positive read pulse is desired, V_1 is set so that application of the gating pulses causes T_1 to turn on, opening the read section of the gate, and thus allowing negative read pulses to appear as positive pulses at the selected output. At the same time V_2 is set so that T_2 is not turned on by the gate pulse; thus the write half of the gate is closed. If a negative write pulse is desired at the output, the state of the bistable multivibrator controlling V_1 and V_2 is changed, and the levels of V_1 and V_2 are interchanged. T_2 is now turned on by the gate pulse, opening the write section of the gate, and negative pulses applied to the write bus appear as negative output pulses. Since the levels of V_1 and V_2 have been interchanged, T_1 is not turned on by the gating pulse and the read section of the gate is closed. The purpose of opening only one side of the gate at a time is to provide efficient operation of the pulse transformer and pulse generators. If both sides of the gate were opened by the application of the gating pulse, the unused primary would be connected to ground through the internal impedance of the pulse generator causing a decrease in gate efficiency.

The transistors employed in the gate are 2N44 *p-n-p* junction transistors. A gating pulse current of approximately 5 ma is used to drive the base of the selected transistor. For simple scanning, the gate has a unity output-to-input ratio for 1:1 transformers; *i.e.*, a negative pulse of 10 volts applied to the read or write bus appears as a 10-volt output pulse. Output impedance of the gate is approximately 120 ohms. Fig. 9 is a photograph of a gate assembly; two complete gates are mounted on each plug-in card. Fig. 10 shows the waveform of a read and write pulse taken at the output of one of the transistor gates.

For bias scanning, operation of the gate is somewhat different and output-to-input ratio is decreased. For this type of operation, biases V_1 and V_2 are initially set at levels different from those used in simple scanning. If a positive read pulse is desired, V_1 is set so that the read section of the gate is normally closed and opens only with the application of gating pulse. V_2 is set so that the write section of *all* gates is normally open; *i.e.*, T_2 is on. To realize a positive read pulse, a negative pulse of amplitude V' is applied to the read bus coincident with the application of a negative pulse of amplitude V'/β to the write bus.

Since both sections of the gate are open, a positive output of $\alpha[V'-(V'/\beta)]$ appears at the output of the selected gates where α takes in the efficiency of the system. At all other column gates, outputs of $-V'/\beta$ occur. For a ratio of V to V/k, V' and β must be adjusted such that

[6] J. Bethke, "New applications for beam switching tubes," *Electronics*, vol. 29; April, 1956.

[7] J. J. Ebers and J. L. Moll, "Large-signal behavior of junction transistors," PROC. IRE, vol. 42, pp. 1761–1772; December, 1954.

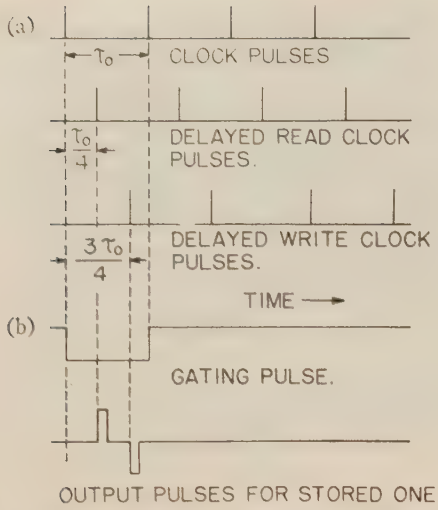


Fig. 11—Pulse sequence for 10×10 matrix scanner.

$$V = 2\alpha\left(V' - \frac{V'}{\beta}\right) \tag{2}$$

and

$$\frac{V}{k} = \alpha\left(V' - \frac{V'}{\beta}\right) - \frac{V'}{\beta}.^{8} \tag{3}$$

Solving for β,

$$\beta = \frac{k(\alpha + 1) - 2\alpha}{\alpha(k - 2)}. \tag{4}$$

If a negative write pulse is desired, the state of the control bistable multivibrator is changed, interchanging the levels of V_1 and V_2 and thereby opening all read gates and allowing a negative write pulse output only where coincidence between a gating pulse and a write pulse occurs. In this manner, pulses of amplitude $\pm V/k$ appear on the unselected cross points of the selected row and column.

Since the type of scanning described employs destructive readout, a method for restoring the information to matrix is incorporated into the scanner. Delay networks are included in each pulse channel such that the clock pulses arrive at the inputs to the read and write control gates as shown in Fig. 11. Under read-restore operation the read gate is normally open and negative read pulses are applied to the selected cross points. If a "1" is detected in a particular cross point, the "1" output from the readout circuit triggers the bistable multivibrator controlling the read and write gates and opens the write gate allowing the delayed write clock pulse to trigger the write generator. Since the gating pulse is still being applied to the row and column gates, a positive write pulse appears across the original storage condenser. The "1" output from the readout circuit also triggers a delay multivibrator which returns the system to read operation. Thus, if a "1" is detected in the selected cross point a positive write pulse restores the storage capacitor to its standard "1" state, allowing a particular pattern to be recalled as many times as desired.

[8] The $-V'/\beta$ term is not multiplied by α since the unselected gates have a unity output-to-input ratio.

Fig. 12—10×10 matrix assembly.

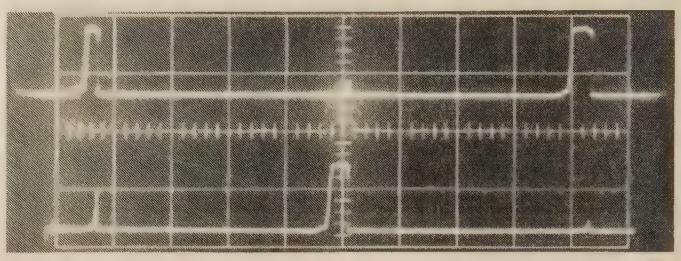


Fig. 13—Matrix output waveforms (10 μsec and 5 volts per large division).

The equipment in its present form operates satisfactorily from zero to 22 kc. Output amplitude from row and column gates is limited to a maximum of 20 volts, giving a total maximum operating voltage of 40 volts. The speed of the device is limited by the transistors used. If fast switching transistors are used in the row and column gates, clock repetition rates of approximately 0.5 mc are possible.

The row and column gates are so designed that only a rough selection of transistors is necessary. When the gating pulse is applied to the base of the grounded emitter switch and turns the switch on, the impedance between collector and emitter drops to a few ohms. This resistance is effectively in series with the internal impedance of the pulse generator. Since the internal impedance of the pulse generators is approximately 100 ohms, a wide variation in "on" resistance can be tolerated without causing noticeable variation in output pulse amplitudes.

Fig. 12 is a photograph of a 10×10 ferroelectric matrix assembly; each "can" contains one ferroelectric cell. Row leads are printed on one side of the card while column leads are printed on the opposite side. Fig. 13 shows a portion of the output waveform from the readout circuit of Fig. 7 for a 1010 · · · and a 0101 · · · stored pattern.

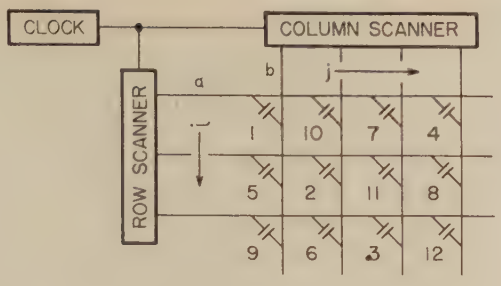


Fig. 14—3×4 rectangular matrix.

Rectangular-Matrix Scanning

A further reduction in electronic circuitry per bit of information is gained by the use of rectangular or non-square matrix arrangements. A 3×4 matrix is shown in Fig. 14. Column and row scanners are driven at the same repetition rate and deliver $\pm V/2$ to the column leads and $\mp V/2$ pulses to the row leads. Assume that the column and row scanners initially start from the column and row leads labeled *a* and *b*. Since both scanners run at the same repetition rate, the matrix will be scanned in cyclic fashion in the order indicated by the numerals on the figure. Note that the row scanner is not required to "hold" on any one particular row lead for a relatively long period of time as is the case in square-matrix scanning where one scanner is driven at a rate equal to the clock rate divided by the number of rows (or columns).

Rectangular-matrix scanning selects every cross point in cyclic fashion of any m-by-n matrix when m and n are chosen such that no common divisor exists (other than one). If a common divisor λ exists, then only $(m\times n)/\lambda$ of $m\times n$ cross points are cyclically scanned. This restriction eliminates 2×4, 4×6, 3×9, etc., matrices.

A circuit, suitable for 9×10 rectangular-matrix scanning, is shown in Fig. 15. Here the outputs from the two beam switching tubes are used to switch the ferroelectric capacitors directly rather than to control gates connected to separate pulse generators as in Fig. 7. One switching tube is connected as a "nine" counter and the other as a decimal (ten) counter, both running at the same clock rate. Outputs are taken from each target through the pulse transformers shown. To obtain both positive and negative pulses across the storage cells, the differentiating properties of a pulse transformer are utilized. As shown in Fig. 15, the lower end of the primary of all transformers is grounded and the upper end is connected to the targets of the beam switching tubes.

The transformer is designed so that saturation occurs in the time interval during which the electron beam rests on a particular target. The diodes $D_1, D_2, \cdots, D_n$ and the transistor switch T control the collapse of the magnetic field of the transformer as the electron beam switches off a given target. The circuit is normally in a reading mode and the cathodes of $D_1, D_2, \cdots D_N$ grounded through the transistor I; thus only positive half pulses are applied to the horizontal matrix wires and negative half pulses to the vertical matrix wires. To

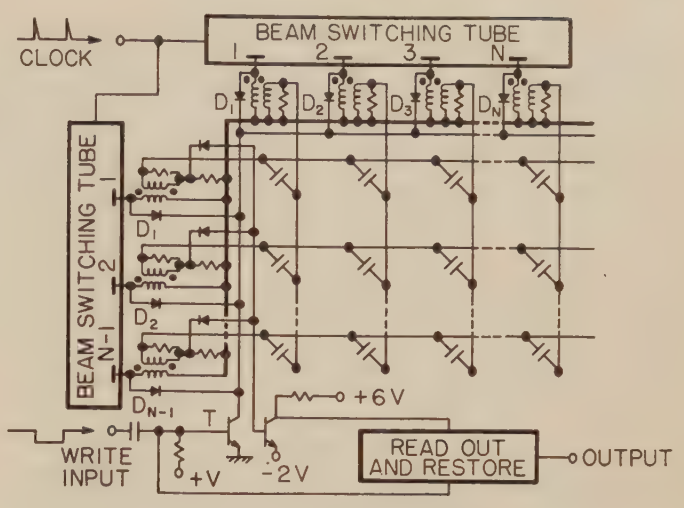


Fig. 15—9×10 matrix scanner.

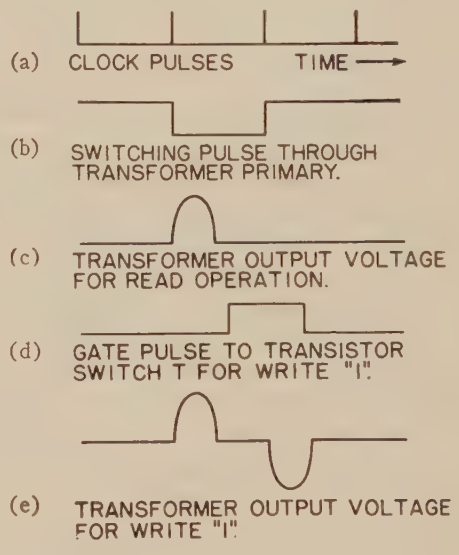


Fig. 16—Pulse sequence for 9×10 matrix scanner.

write a binary "1" into the matrix, the switch T is opened after a given transformer has become saturated and is held open until the electron beam has switched to the next position. Diodes $D_1, \cdots, D_n$ are thus disconnected from ground; the collapsing field of the selected transformer thus produces a negative half pulse on the corresponding horizontal matrix wire and a positive half pulse on the corresponding vertical matrix wire. Fig. 16 shows the sequence of pulses used to derive a positive read pulse and a negative write pulse.

This system of obtaining positive read and negative write pulses is applicable only to rectangular scanning. In the pulse sequence of Fig. 16, it should be noted that a write pulse for the nth clock pulse occurs almost simultaneously with the read pulse for the $(n+1)$th clock pulse. However, since rectangular scanning is being used, the selected cross point for the nth clock pulse is ij while the selected cross point for the $(n+1)$th clock pulse is $i+r, i+s$ where r and s are nonzero integers. Thus, the simultaneous application of read and write

pulses does not occur on the same row or column or through the same transformer.

This system is also applicable to a read-restore type of operation. For this mode, the transistor switch T is controlled through a delay network by the output signals from binary "1"s stored in the matrix. Fig. 17 is a photograph showing a complete column scanner for a 9×10 matrix.

Conclusion

Characteristics of the systems described can be summarized as follows.

Linear Scanning

This configuration is applicable to small-size memories since the amount of electronic driving circuitry per bit of information is high. The quality of the ferroelectric storage element is not critical and large one-to-zero signal ratios are easily obtained.

Square-Matrix Scanning

With the ferroelectric materials now available, this mode of operation is also limited to relatively small matrices, although the size of the memory may be relatively large since the system is easily adaptable to the parallel operation of many small matrices. The size of a square matrix can be increased by a factor of approximately three through the use of pulse bias scanning. A further improvement in matrix size may be also made by introducing additional nonlinearity into the matrix cross points by combining ferroelectric storage elements with the nonlinear characteristics of diodes or transistors.[9] At the present time, this is economically unfeasible for large-scale memories.

Rectangular-Matrix Scanning

For small-size memories, employing sequential selection, rectangular-matrix scanning reduces the amount of electronic circuitry per bit, in that the system described combines both scanning and switching in a single operation.

[9] A paper describing this technique is in preparation.

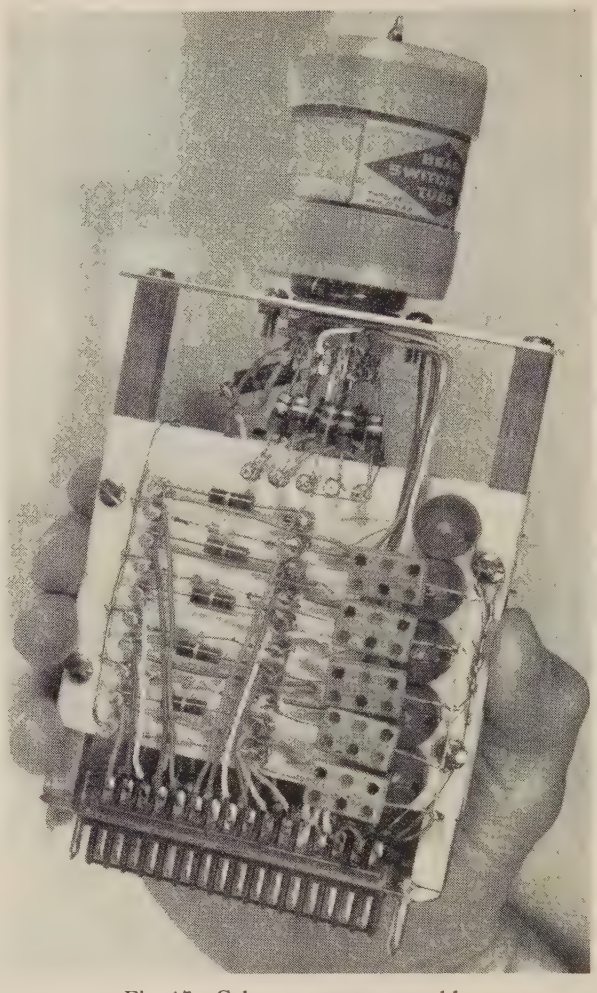


Fig. 17—Column scanner assembly.

Ultimately, the choice of configuration and scanning depends on the application, size of the memory, access time desired, and quality of the element used.

Acknowledgment

The authors wish to acknowledge the assistance of Fredrick D. Weekes, who designed and tested a portion of the apparatus, and George Meszaros, who constructed the equipment.

A Transistorized Four-Quadrant Time-Division Multiplier with an Accuracy of 0.1 Per Cent*

HERMANN SCHMID†

Summary—**This article describes a four-quadrant time-division multiplier with an over-all accuracy of better than 0.1 per cent of full scale. The circuit is independent of the transistor characteristics, requires no complicated balancing adjustments, exhibits excellent stability and uses only simple, noncritical circuitry. The maximum output voltage is 10 v when both input voltages are 10 v.**

Introduction

OVER the past decade, the time division multiplier has become a very popular device in analog computing techniques. Several versions of this multiplier have been described recently in the literature, from a slow, simple, relay type to a high precision unit occupying several panels of a rack.[1–4]

The multiplier described here is different in that it uses transistors as electronic switches with unusual accuracy. Whereas the usual procedure of employing transistors is to substitute them for vacuum tubes, in this application the transistor characteristics are used in a manner not possible with tubes. It is precisely these characteristics which make this multiplier possible. The main effort in this report is therefore directed to elaborate on the electronic transistor switch.

Basic Operation of the Multiplier

The operating principle of this multiplier may be understood by reference to the block diagram of Fig. 1. Three basic units can be recognized from it: 1) the conversion unit, 2) the transistor switch, and 3) the filter unit.

The Conversion Unit

The conversion unit, shown within the dashed lines of Fig. 1, consists of a dc amplifier, the sawtooth oscillator, the squaring (limiting) amplifier, a transistor switch, and a filter. V_y, one multiplication variable, and V_f, the feedback voltage, produce an error voltage which is amplified by the dc amplifier and used to bias the sawtooth oscillator. Thus the mean level of the sawtooth wave is shifted about ground proportional to $V_y + V_f$. The squaring amplifier has the characteristic of amplifying only a slice of the sawtooth (± 10 mv about ground) into a rectangular wave. The amplitude of the rectangular wave is determined by the supply voltage of the squaring amplifier and the pulse width by the width of the sawtooth in the slice to be amplified, which in turn depends on the bias applied to the sawtooth oscillator. The squaring amplifier provides push-pull output.

This push-pull signal controls not only the bases of the transistor switches 1, 2, 3, etc., but also the bases of the switch in the conversion unit, which limits the amplitude of the rectangular wave very accurately to $\pm V_r$, the reference voltage. The filter following the switch provides the average of the rectangular wave which is proportional to $V_r V_y$, identified as V_f. This closes the loop of the conversion unit, the sole purpose of which is the conversion of V_y from a dc voltage to a time-modulated signal. Fig. 2 illustrates the biasing of the sawtooth wave as well as the variation of the pulse width, t, with respect to V_y. When $V_y = 0$, the bias voltage, V_b, and the mean level of the sawtooth wave equals zero too. Therefore, the pulse width, t, of the rectangular wave is $T/2$, where T is the total period of the pulse cycle

As V_y becomes more negative, V_b becomes more positive, and thus the pulse width, t, increases. In a similar manner, t decreases when V_y becomes positive.

The Transistor Switch

Ths transistor switch, illustrated in the schematic of Fig. 3, consists of two emitter-to-emitter connected *p-n-p* transistors. The operation of the transistor switch can be symbolized by a relay having a single-pole, double-throw contact. Its main purpose is to limit the amplitude of the rectangular wave to $\pm V_x$, the second multiplication variable, and so produce the product, $K V_y V_x$.

To simplify the description of the operation of the transistor switch, specific values, $V_x = 6$ v, and V_A and V_B varying between ± 10 v, shall be assumed here. In addition, a tabulation of conditions occurring during the various phases of operation is presented in Table I for reference.

With -6 v on the collector of T_1 and $+6$ v on the collector of T_2, transistor T_1 functions as an emitter follower (analog of a cathode follower) and T_2 as load impedance for T_1 as long as the base drive V_A is numerically smaller than 6 v. In other words, the output follows V_A within the region between -6 v and $+6$ v.

When V_A exceeds $+6$ v, current will flow from the output to the base of T_2. This forward biases the emitter-base junction of T_2, and as the collector-base junc-

* Manuscript received by the PGEC, August 27, 1957; revised manuscript received, November 12, 1957.

† Link Aviation, Inc., Binghamton, N. Y.

[1] G. A. Korn and T. M. Korn, "Electronic Analog Computers," McGraw-Hill Book Co., Inc., New York, N. Y., ch. 6; 1956.

[2] K. Chen and R. O. Decker, "Analog multiplying circuits using switching transistors," 1956 IRE Convention Record, pt. 4, pp. 74–80.

[3] R. A. Meyers and H. B. Davis, "Triangular wave analog multiplier," *Electronics*, vol. 29, pp. 182–185; August, 1956.

[4] E. A. Goldberg, "A high accuracy time-division multiplier," *RCA Rev.*, vol. 13, pp. 265–274; September, 1952.

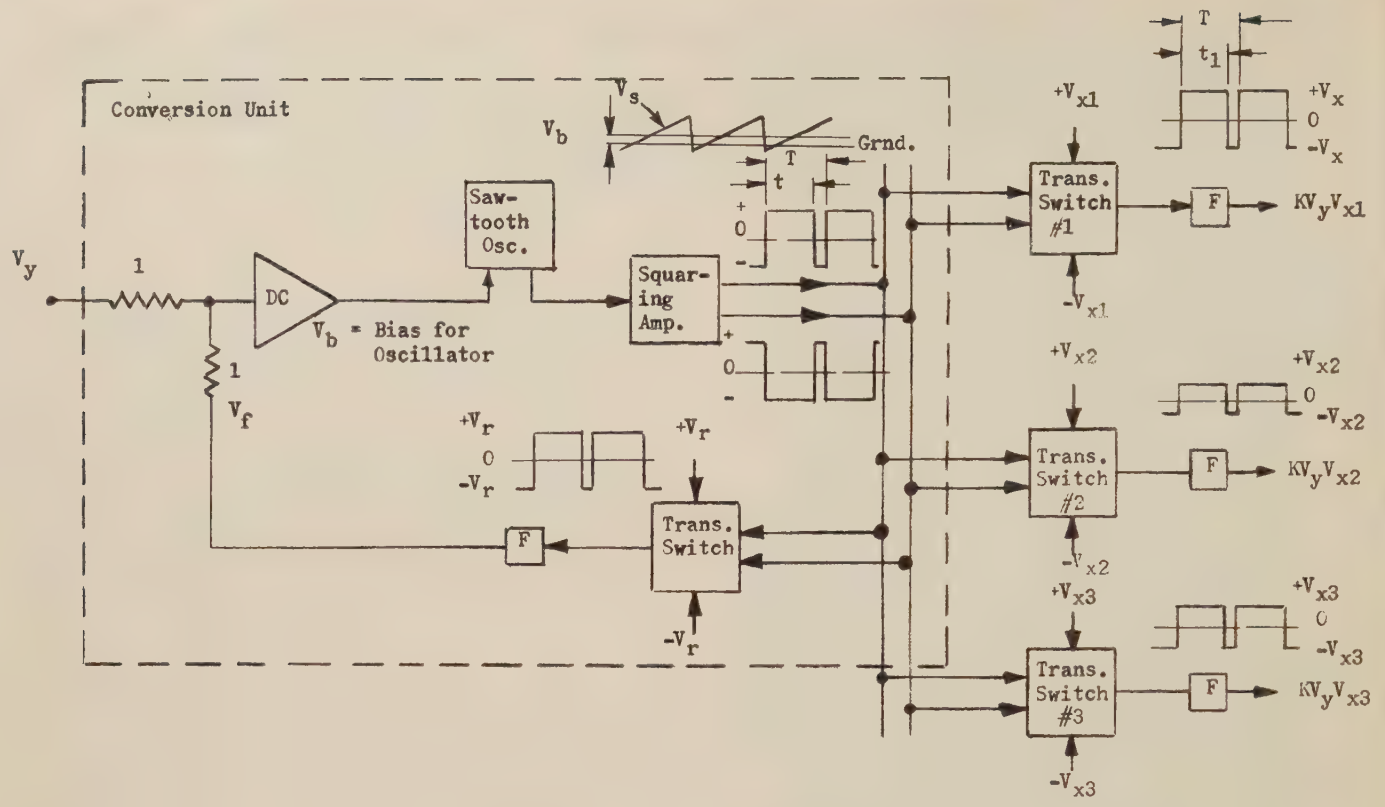


Fig. 1—Block diagram of four-quadrant time-division multiplier.

V_y, V_x = machine variables
V_r = reference dc voltage
F = passive filter
V_f = feedback voltage
V_b = bias for oscillator
Note: circuitry in dashed lines converts V_y into a pulse width t_1.

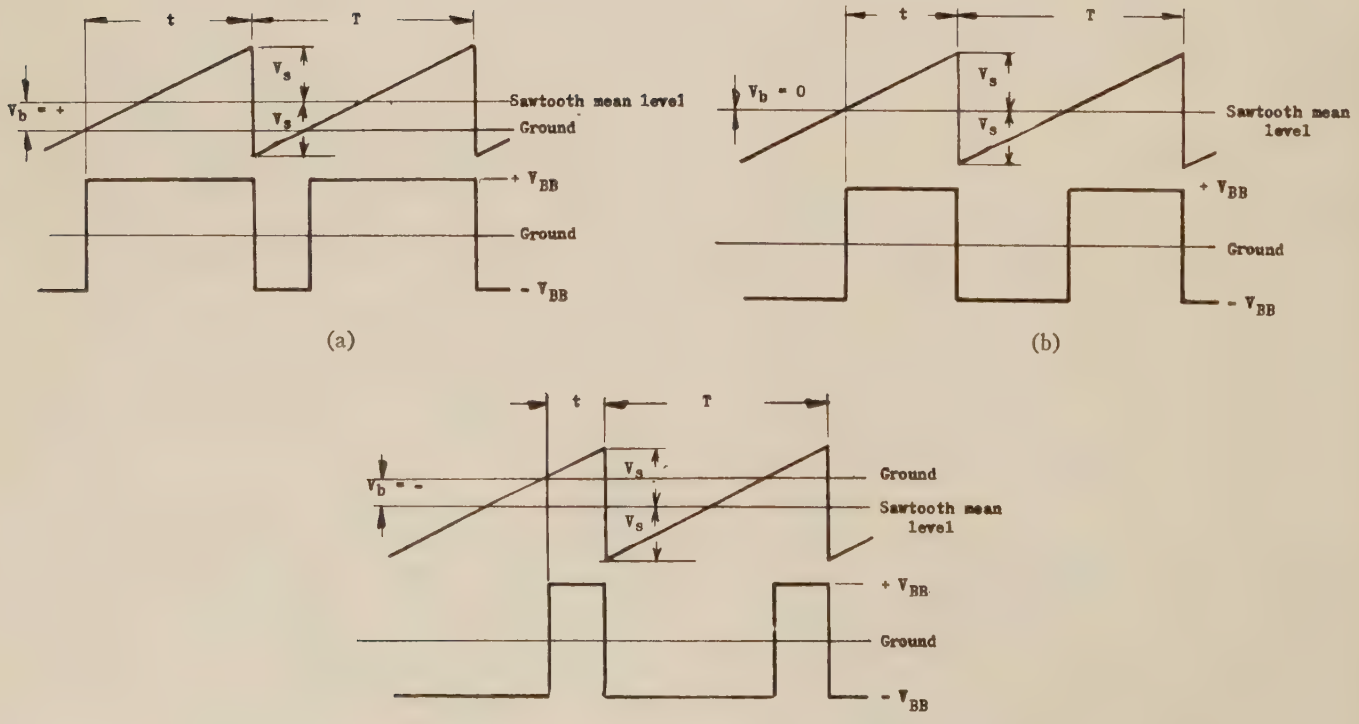


Fig. 2—Variation of pulse width vs V_y. (a) $V_y = -5$ v, (b) $V_y = 0$, (c) $V_y = +5$ v.

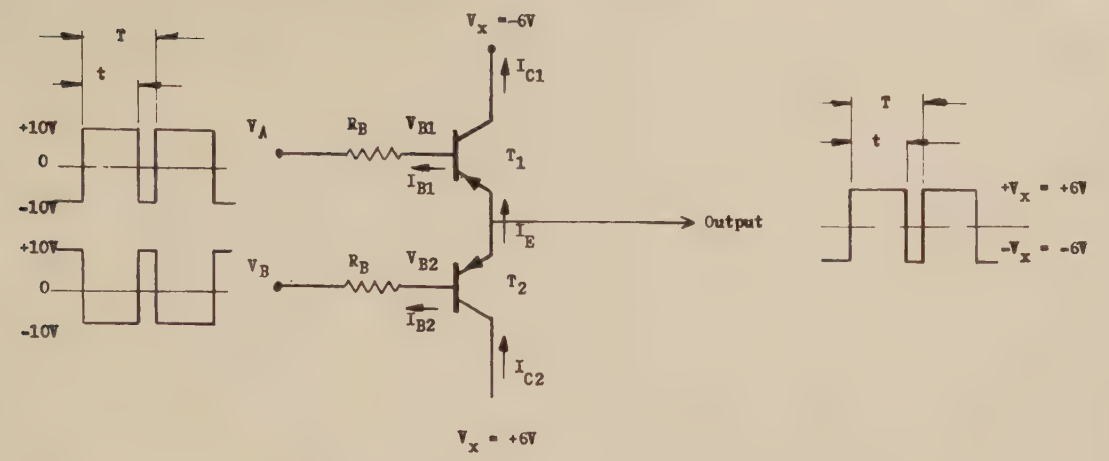
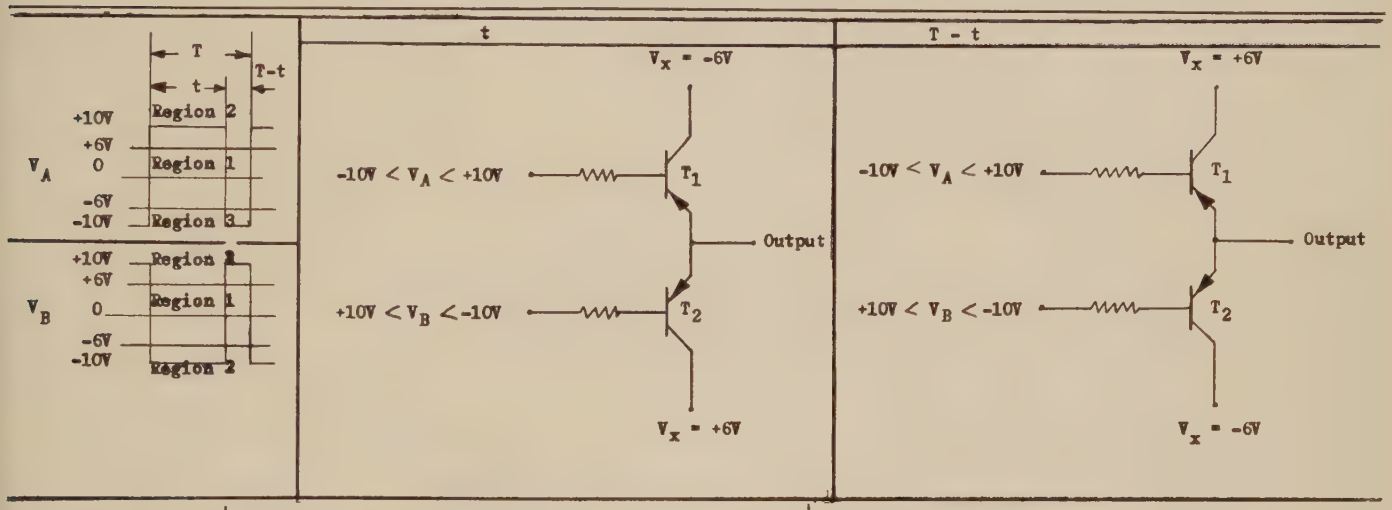


Fig. 3—The transistor switch. Direction of I_E, I_{C1}, I_{C2} is valid only for the collector voltages indicated. When the collector voltages are reversed, the direction of these currents also reverses.

TABLE I

TABULATION OF CONDITIONS OCCURRING IN THE TRANSISTOR SWITCH DURING THE VARIOUS PHASES OF OPERATION



	t	T - t
Region 1: -6 v $< V_A <$ $+6$ v $+6$ v $> V_B >$ -6 v	T_1 functions as emitter-follower. Output follows V_A. T_2 functions as load.	T_2 functions as emitter-follower. Output follows V_B. T_1 functions as load.
Region 2: $+6$ v $< V_A <$ $+10$ v -6 v $> V_B >$ -10 v	Emitter and collector of T_2 are forward biased and thus T_2 conducts. Emitter and collector of T_1 are reverse biased and thus T_1 cut off. Output stays at $+6$ v.	Emitter and collector of T_1 are forward biased and thus T_1 conducts. Emitter and collector of T_2 are reverse biased and thus T_2 cut off. Output stays at -6 v.
Region 3: -6 v $> V_A >$ -10 v $+6$ v $< V_B <$ $+10$ v	Emitter and collector of T_1 are forward biased and thus T_1 conducts. Emitter and collector of T_2 are reverse biased and thus T_2 cut off. Output stays at -6 v.	Emitter and collector of T_2 are forward biased and thus T_2 conducts. Emitter and collector of T_1 are reverse biased and thus T_1 cut off. Output stays at $+6$ v.

tion is already forward biased, T_2 conducts. While T_2 is conducting, T_1 is cut off because its emitter-base junction and its collector-base junction are reverse biased. With T_2 conducting and T_1 cut off, the circuit performs almost like an ideal switch which connects the potential, $+6$ v, at the collector of T_2 to the output.

When V_A is more negative than -6 v, current will flow from the collector of T_1 to the base of T_1. This will forward bias the collector-base juuction and as the emitter-base junction is already forward biased, transistor T_1 conducts. At the same time, V_B is larger than $+6$ v, which means that the collector-base junction as well as the emitter-base junction of T_2 are reverse biased and therefore T_2 is cut off. This provides the other position of the ideal switch, with T_1 conducting and T_2 cut off, and the potential, -6 v, on the collector of T_1 connected to the output.

The inherent symmetry of the switching circuit suggests that the circuit functions in an identical manner when the collector voltages are reversed. The output voltages and the currents (I_C, I_E, I_B) vs the base drive (V_A and V_B) of such a transistor switch are plotted in Fig. 4 for $V_x = \pm 6.3$ v. It can be seen there that the currents are very low (close to zero) when V_A is larger than V_x. In the transition region, where the circuit operates as an emitter follower, I_C and I_E increase from zero at

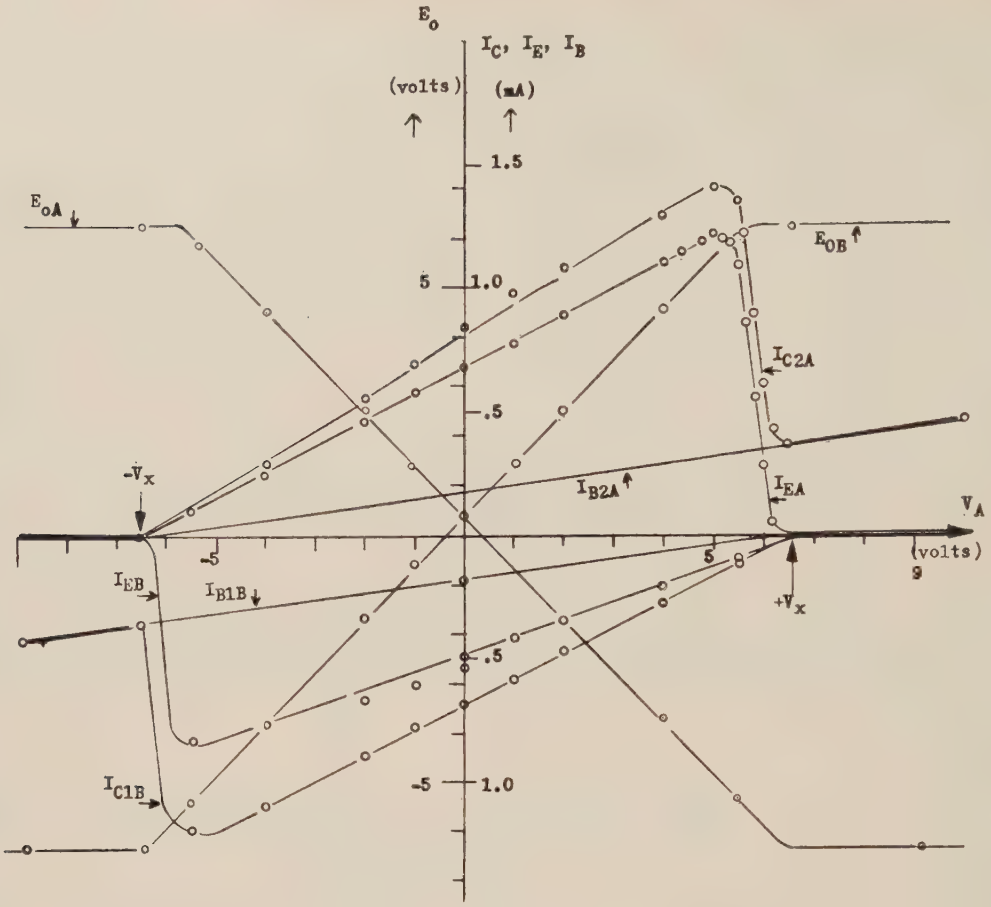


Fig. 4—E_0, I_C, I_E, I_B vs basedrive (V_A). For the transistor switch.
Case A = −6.3 v on T_1 and +6.3 v on T_2.
Case B = +6.3 v on T_1 and −6.3 v on T_2.

one extreme to a maximum shortly before the other extreme is reached, while I_B increases always proportionally with V_A.

It is worth noting that both transistors are connected in the grounded collector configuration. Although this requires more power to control the switch, it provides smaller voltage drops between collector and emitter of the conducting transistor.

The Filter Unit

The filter unit used in this multiplier has the purpose of extracting the dc mean level from the rectangular wave. Its prime requirements are, therefore, to attenuate the carrier frequency to a specified minimum value, to attenuate all frequencies from zero to the upper multiplication frequency as little as possible, and to have a phase shift for all frequencies between zero and the upper multiplication frequency as small as possible. Other requirements are small size and reasonable cost.

DC Analysis of the Conversion Unit

The conversion unit shown in Fig. 1 is nothing but a feedback network with an active element in the feedback loop. Therefore, it behaves and performs like a closed loop circuit and thus can be analyzed like one. The relationship between the pulse width, t, and the bias voltage, V_b, the sawtooth amplitude, V_s, and the repetition period, T, can be seen in Fig. 2.

$$t = \frac{T}{2}\,\frac{V_s + V_b}{V_s} \quad \text{or} \quad \frac{t}{T} = \frac{1}{2}\left(1 + \frac{V_b}{V_s}\right). \tag{1}$$

The voltage, V_f, fed back to the summing point is the mean value of the rectangular wave from the transistor switch, with the amplitude of $\pm V_r$, where V_r is the computation or reference voltage.

$$V_f = -V_r\left(1 - 2\,\frac{t}{T}\right).$$

Substituting t/T by (1),

$$V_f = -V_r\left[1 - \frac{2}{2}\left(1 + \frac{V_b}{V_s}\right)\right] = \frac{V_r V_b}{V_s}. \tag{2}$$

The bias voltage, V_b, is the sum of V_y and V_f multiplied by the gain of the dc amplifier, A. When V_f is replaced by its equivalent in (2),

$$V_b = (V_y + V_f)A = AV_y + A\,\frac{V_r V_b}{V_s},$$

$$V_b = \frac{AV_y}{1 - \dfrac{AV_r}{V_s}}. \tag{3}$$

Finally, the output of the feedback network, namely, the time division $1-2t/T$, can be calculated by referring to (1) and replacing V_b by (3),

$$1-2\frac{t}{T}=1-\frac{2}{2}\left(1+\frac{V_b}{V_s}\right)=\frac{\dfrac{AV_y}{1-AV_r/V_s}}{V_s}$$

$$=\frac{AV_y}{V_s-AV_r}. \tag{4}$$

Eq. (4) can be simplified further by assuming $AV_r \gg V_s$,

$$1-2\frac{t}{T}=-\frac{V_y}{V_r}. \tag{5}$$

From (5), it can be seen that the output $(1-2t/T)$ is directly proportional to V_y and inversely proportional to V_r. Since V_r is constant, the output varies only with V_y. When the gain of the dc amplifier is high, the output is independent of the amplitude, linearity, and frequency of the sawtooth wave. Since this is so, the sawtooth waveform can be of very poor quality; in fact, it can even be a sine wave without introducing a noticeable error. The high gain feedback network will, for either waveform, produce a pulse width at the output of the squaring amplifier that is directly proportional to the input variable V_y. Changes in V_r appear as direct errors at the output. However, since V_r is the computing voltage, which is also used as reference throughout the system, no relative error results. The circuit will function as a divider, with an accuracy of better than 0.5 per cent when V_y is kept constant and V_r varied.

Design Considerations on the Transistor Switch

Switching with transistors has been described at some length in the literature during the past few years.[5-7] In spite of this, it is felt worthwhile to elaborate on this particular application of transistors, since the problems encountered here differ in several respects from those described in the literature mentioned. In the design of the transistor switch for the time-division multiplier, the following requirements became apparent.

1) The switch should be able to handle large voltages (0 to 20 v or higher). To satisfy this requirement, it is necessary to select transistors with high V_{CB}, V_{EB}, and punch-through voltage. While it is easy to find transistors with $V_{CB} \geq 40$ v, it seems that transistors with V_{CB}, V_{EB}, and punch-through voltage larger than 40 v are not yet available. All of these breakdown voltages are affected by the external base resistance; the larger R_B, the smaller the breakdown voltages and vice versa.

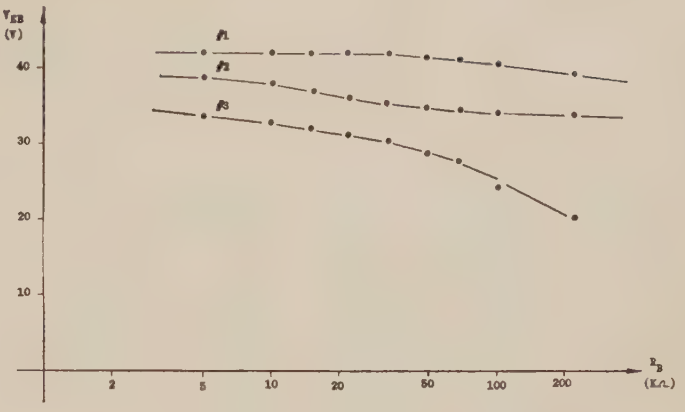


Fig. 5—Emitter-base breakdown voltage vs base resistance for three 2N43 transistors.

Emitter-base breakdown characteristics vs base resistances for three 2N43 transistors are plotted in Fig. 5. It follows from the above that for the maximum dynamic range of the switch, the external base resistance should be as small as possible.

The peak emitter and collector currents flowing through the transistors in the transition region, as shown in Fig. 4, are determined by the amount of base current flowing in the transistor functioning as an emitter follower. This I_B is again proportional to the external base resistance. The larger R_B, the smaller I_B, I_E, and I_C. As these currents are flowing only during a certain time, they create ripple on the supply voltage to the switch, namely $\pm V_z$. It is therefore advantageous to keep these currents as small as possible. This, however, is directly contrary to the first requirement and, as usual, a compromise is the solution. A value of 27 k has therefore been chosen for the breadboard.

The transistors used for the breadboard model of this multiplier are GE 2N43 with minimum V_{CB} and V_{CE} specified at 45 v and 20 v, respectively. Measurements of V_{EB} over a large range of base resistance, for a lot of 24, yielded emitter breakdown voltages in excess of 30 v.

2) The voltage drop across the switch should be very small when conducting. The voltage drop between collector and emitter, V_{CE}, has been determined by Ebers and Moll[7] for the grounded emitter configuration as

$$V_{CE}=k\ln\frac{\alpha_I\left(1-\dfrac{I_C}{I_B}\dfrac{1-\alpha_N}{\alpha_N}\right)}{1+\dfrac{I_C}{I_B}(1-\alpha_I)},$$

and for the grounded collector configuration as

$$V_{CE}=k\ln\frac{\alpha_N\left(1-\dfrac{I_E}{I_B}\dfrac{1-\alpha_I}{\alpha_I}\right)}{1+\dfrac{I_E}{I_B}(1-\alpha_N)}.$$

where

[5] Bright, "Junction transistors used as switches," *Trans. AIEE (Commun. and Electronics)*, vol. 17, pp. 111–121; March, 1955.

[6] Trousdale, "Symmetrical transistor as a bilateral switching element," *Trans. AIEE (Commun. and Electronics)*, vol. 26, pp. 400–403; September, 1956.

[7] J. J. Ebers and J. L. Moll, "Large-signal behavior of junction transistors," Proc. IRE, vol. 42, pp. 1761–1772; December, 1954.

TABLE II

ACCURACY MEASUREMENTS ON MULTIPLIER NO. 407

V_x \ V_y	−10 v	−8 v	−6 v	−4 v	−2 v	−1 v	−.5 v	0 v	+.5 v	+1 v	+2 v	+4 v	+6 v	+8 v	+10 v
+10 v	10.000	8.008	6.006	4.004	2.003	1.001	.500	−.002	.500	.99	2.000	4.001	6.002	8.000	9.992
+8 v	7.993	6.406	4.807	3.206	1.604	.805	.406	−.006	.395	.795	1.594	3.196	4.798	6.398	7.997
+6 v	6.000	4.806	3.606	2.405	1.207	.605	.305	−.006	.296	.595	1.193	2.394	3.596	4.793	6.000
+4 v	3.998	3.202	2.403	1.604	.803	.405	.204	−.005	.196	.396	.795	1.595	2.395	3.196	3.998
+2 v	2.000	1.600	1.200	.800	.400	.201	.101	−.004	.098	.198	.398	.797	1.198	1.599	2.000
+1 v	.999	.798	.600	.399	.201	.100	.050	−.002	.049	.099	.198	.398	.598	.799	.997
+.5 v	.500	.400	.300	.199	.100	.050	.025	−.002	.025	.050	.100	.201	.300	.400	.502
0 v	.001	.001	.001	.001	.001	.001	.001	−.001	.001	.001	.001	.001	.001	.001	.001
−.5 v	.501	.400	.300	.200	.100	.050	.025	−.001	.025	.050	.100	.199	.300	.400	.499
−1 v	1.000	.800	.600	.399	.200	.100	.050	−.002	.050	.100	.200	.400	.599	.799	1.000
−2 v	2.000	1.599	1.200	.800	.400	.198	.100	−.002	.100	.201	.400	.800	1.198	1.600	2.000
−4 v	3.999	3.195	2.396	1.596	.798	.396	.198	−.003	.201	.401	.803	1.600	2.400	3.199	4.002
−6 v	5.996	4.792	3.592	2.395	1.196	.595	.297	−.004	.303	.602	1.204	2.401	3.600	4.800	6.002
−8 v	7.995	6.393	4.794	3.195	1.595	.796	.396	−.004	.403	.801	1.600	3.202	4.800	6.403	8.002
−10 v	9.999	7.999	5.995	3.994	1.996	.996	.497	−.002	.52	1.001	2.002	4.003	6.004	8.000	9.995

Output voltage E_0 in volts

Note: All voltages in the first and third quadrant are positive.
All voltages in the second and fourth quadrant are negative.

V_{CE} = voltage drop between collector and emitter.
I_E = emitter current.
I_B = base current.
I_C = collector current.
k = 0.26 v at 25°C.
α_N = forward or normal amplification factor.
α_I = inverse amplification factor.

From these formulas it can be seen that for I_C approaching zero, V_{CE} is proportional to ln α_I in the grounded emitter configuration and for I_E approaching zero, V_{CE} is proportional to ln α_N in the grounded collector configuration. Since for all unsymmetrical transistors (areas of collector greater than area of emitter), $\alpha_N > \alpha_I$, the grounded collector configuration will provide smaller voltage drops (V_{CE}) between collector and emitter.

With 2N43 transistors, connected as shown in Fig. 3, V_{CE}'s of less than 1 mv have been obtained over a range of ±20 v of switching voltage. This was better than the V_{CE}'s obtained with symmetric switching transistors whose maximum amplification factors ($\alpha_N = \alpha_I$) are smaller than α_N of the unsymmetrical transistor.

3) The switching rate should be high. The frequency response of the transistor switch should be such that the rectangular wave used as a carrier will not be distorted. As the carrier is a square wave, the frequency cutoff of the transistor should be approximately 100 times higher than the fundamental frequency of the carrier.

For the breadboard tested, a carrier frequency of 1 kc was chosen. As the alpha cutoff of the 2N43 transistors is of the order of 1 mc, no deterioration of the square wave was noticed. The maximum switching rate of the transistor switch appears to be about 2 kc.

THE STATIC PERFORMANCE OF THE MULTIPLIER

A typical series of measurements, in which the product (KV_xV_y) is recorded for various values of V_x and V_y, is illustrated in Table II. It is believed that a tabulation of this kind is more informative than a graphical representation of these measurements, as it not only shows the output voltage of the multiplier more accurately but also defines explicitly the absolute error of each reading. From Table II, it can be seen that the maximum absolute error is smaller than ±10 mv. With a maximum output of 10 v (full scale), this means an over-all accuracy of ±0.1 per cent of full scale over all four quadrants, while the accuracy in any one quadrant may be better than ±0.05 per cent of full scale.

Since, in time-division multipliers, the maximum output is determined only by the multiplication variable on the switch, $\pm V_x$, the constant, K, can be obtained from the relation $K = 1/V_{y\ \max}$ (assuming that $V_r = V_{y\ \max}$ and the summing resistors equal). With $V_{x\ \max} = 10$ v and $V_{y\ \max} = 10$ v, the maximum output is also 10 v and therefore $K = 0.1$.

The absolute error vs $\pm V_y$, with $\pm V_x$ as a parameter, is shown in Fig. 6. It can be seen there that the absolute error decreases with decreasing V_x. The irregularity in the curves leads to the assumption that the measuring accuracy is not much better than ±2 mv so that errors plotted in Fig. 6 are the errors of the multiplier ± the measuring errors. The accuracy to which these measurements can be repeated is almost the same as the measuring accuracy.

The dynamic range of the multiplier is, at present, limited by the breakdown voltages of the transistors. With 2N43, where the maximum value for V_x lies at approximately 15 v, and V_{CE} is of the order of 1 mv, a dynamic range of 15,000 can be obtained.

The time and temperature stability of this multiplier is excellent as the output is derived from a digital device (transistor switch) which is controlled by a closed loop system. An increase in temperature of 20°C resulted in an error of less than 0.1 per cent of full scale.

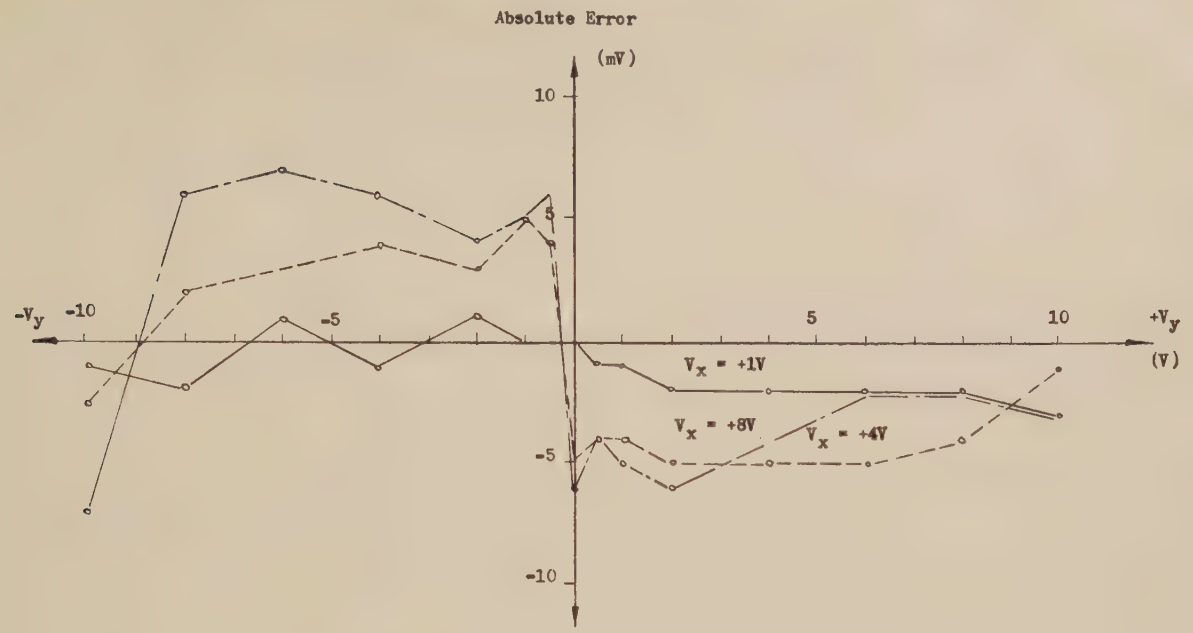


Fig. 6—Absolute error vs $\pm V_y$ with V_x as parameter (Full scale = ± 10 v).

The zero offset voltage depends on how equal are:

1) The voltage drops of the transistors in the closed condition.
2) The amplitudes and pulse areas of the positive and negative parts of the base drive signals, V_A and V_B.
3) The magnitudes of the $+V_x$ and $-V_x$ multiplication variable.

The variables, $+V_x$ and $-V_x$, were derived for the breadboard from dc operational amplifiers; therefore, no appreciable offset voltage resulted from these sources. This is shown in the horizontal row, $V_x = 0$, in Table II. However, in spite of equal amplitudes of the base drive signals, V_A and V_B, a maximum offset of 6 mv is listed in the vertical column, $V_y = 0$, in Table II.

The data presented so far discuss only the static performance. The dynamic performance as a function of the multiplication frequency is, nevertheless, of equal importance. Experimental data on the dynamic performance of this multiplier is not available yet; however, consideration will show that the characteristic frequency limitations of this multiplier do not differ greatly from other electronic time-division multipliers.

New Applications of an Electronic Function Generator*

RAJKO TOMOVICH†

Summary—In previous papers a new technique for performing in a single electronic computing unit all nonlinear mathematical operations in a differential analyzer was described.

The field of application of this technique is extended to include the generation of functions of several variables.

Introduction

In previous papers a new technique for performing nonlinear mathematical operations in analog computers has been described.[1,2] The electronic function generator based on this technique represents, in fact, a simple and versatile computing unit performing all nonlinear operations in an electronic differential analyzer.

The purpose of this paper is to show that the field of application of this technique can be extended to include the generation of functions of several independent variables.

In order to facilitate the explanations, a short review of the principles of the function generator is presented in a suitable form.

Principles of the Function Generator

The starting point of our universal function generator is

$$e = v(x) \cdot f[g(x)]; \tag{1}$$

x is the independent variable. It is easily seen that all nonlinear operations in a differential analyzer, such as function generation, multiplication, division, etc., can be derived as special cases of (1).[2] The network performing transformation (1) on the two input functions $v(x)$ and $g(x)$ in a finite number of points x_n is given in Fig. 1.

According to (1) it is assumed that the potentiometers Q are set in a linear relation

$$u_n - u_{n-1} = \Delta u = \text{const.}$$

and that the common voltage supply is fixed. By varying $f(n)$, the function stored on the potentiometers P, as well as the inputs $v(x)$ and $g(x)$, different nonlinear mathematical operations in the differential analyzer can be performed.

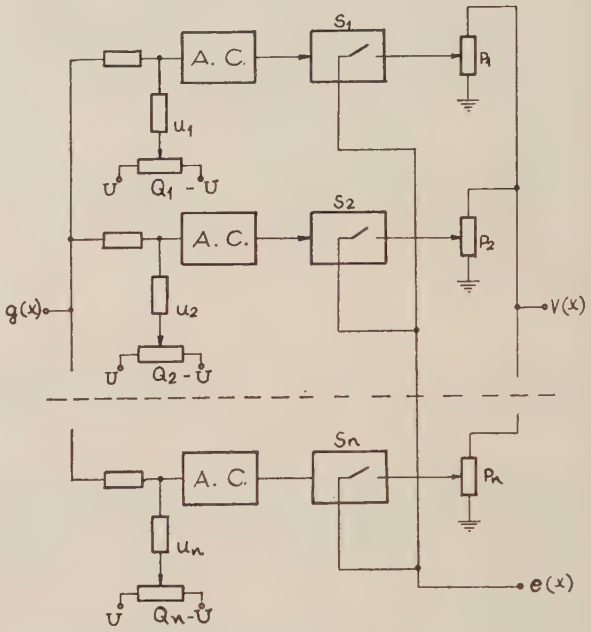


Fig. 1—AC amplitude comparators closing switches S at the instants of equality of $g(x)$ and the corresponding bias voltages. Network output is e.

Nonequidistant Reference Voltages of Amplitude Comparators

Let us consider the case when Δu is not constant but the reference voltages of the amplitude comparators follow an arbitrary law

$$u = h(n).$$

In practice, no difficulties arise since the reference voltages of the amplitude comparators are adjusted by potentiometers Q.

The amplitude comparators of Fig. 1 will now produce a series of time modulated pulses closing the switches S as determined by

$$h(n) = g(x_n)$$

or

$$n = h^{-1}[g(x_n)]. \tag{2}$$

Graphical solution of the above equation is given in Fig. 2.

Since the functional relation stored on the potentiometers P is set as

$$f(n),$$

(1) now takes the more general form

* Manuscript received by the PGEC, October 11, 1957.

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[1] R. Tomovich, "A universal unit for the electrical differential analyser," *J. Franklin Inst.*, vol. 254, pp. 143–151; August, 1952.

[2] R. Tomovich, "A versatile electronic function generator," *J. Franklin Inst.*, vol. 257, pp. 109–120; February, 1954.

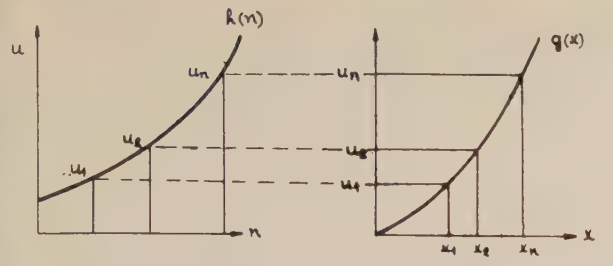

Fig. 2—Determination of intersection points of $h(n)$ and $g(x)$.

$$e = v(x) \cdot fh^{-1}[g(x)] \tag{3}$$

aking into account (2).

In order to present in a clear way all the possibilities f the network in Fig. 1, we shall use for its representaion the block diagram of Fig. 3.

A few examples will be given to demonstrate how (3) an be exploited in the differential analyzers.

One interesting application is the generation of comosite functions. Let us take

$$v(x) = \text{const.}$$
$$f(n) = \sin n$$
$$h(n) = \sqrt{n}.$$

nput $g(x)$ is arbitrary. The output of the function genrator is, according to (3),

$$e = k \cdot \sin [g(x)]^2$$

where k is the scale factor.

As seen, the function generator will perform in one nit the squaring of $g(x)$ and function generation proper The conventional types of function generators, however, would require an additional squarer for the case in question.

Another way of using (3) is also of interest. The function generator is set as follows:

$$f(n) = n$$
$$h(n) = \sqrt{n+1}.$$

The output is

$$e = k \cdot v(x) \cdot [g(x)^2 - 1].$$

Applying this result to the solution of van der Pol's equation

$$\frac{d^2y}{dx^2} + k \cdot (y^2 - 1) \frac{dy}{dx} + y = 0$$

on the differential analyzer, the advantages of the function generator are evident. The block diagram of van der Pol's equation is given in Fig. 4 if the differential analyzer is provided with the electronic function generator of this type. Instead of a squarer and a multiplier, only one unit is needed. All sign considerations are taken into account when setting the function generator so that no additional equipment is required.

The above technique is very convenient for repetitive differential analyzers having a limited accuracy but demanding components with good frequency rseponse. Very compact, simple, and versatile repetitive installations can thus be built. Experience has shown that for the majority of applications the number of points to be set in $f(n)$ and $h(n)$ is

$$5 \leq n \leq 15$$

taking into account that a linear approximation of the integrated output is possible.[3]

Regarding $h(n)$, it should be added that the method best suited for monotonic functions is important in practice as seen from the given examples. The restriction, however, can be offset by various means. For instance, amplitude comparators reacting on

$$\frac{dg(x)}{dx} > 0$$

and

$$\frac{dg(x)}{dx} < 0$$

can be used separately.

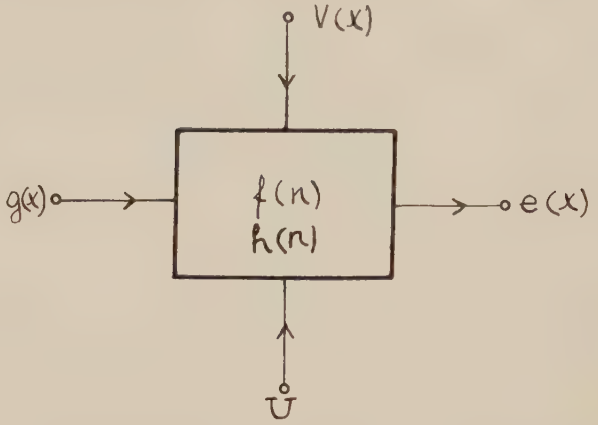

Fig. 3—Block diagram of the function generator. Functions $v(x)$, $g(x)$ are inputs; relations $f(n)$, $h(n)$ are set on the potentiometers P and Q.

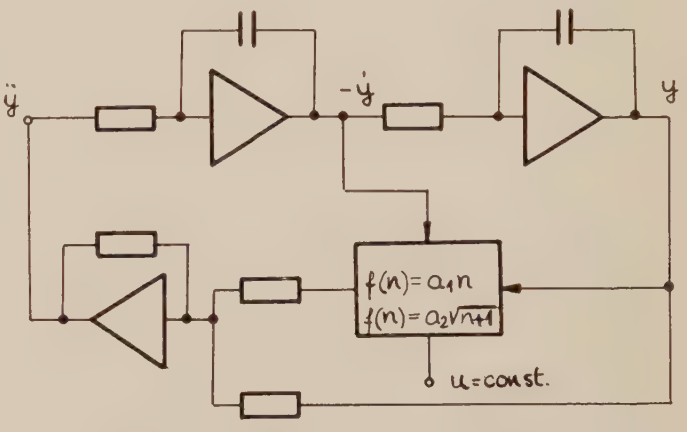

Fig. 4—Block diagram of van der Pol's equation.

[3] R. Tomovich, "Sur une methode augmentant la précision d'un générateur de fonctions," *Proc. Internatl. Assn., Analog Computation, Bruxelles*, pp. 121–123; 1956.

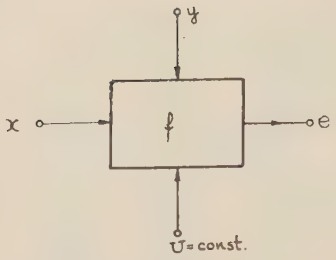

Fig. 5—Generation of $e=y\cdot f(x)$.

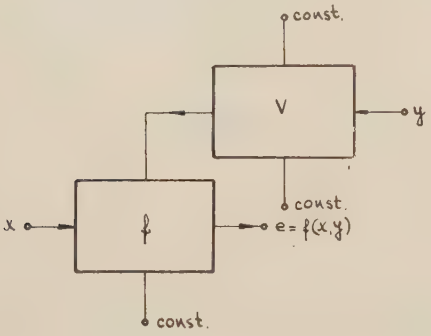

Fig. 6—Generation of $e=v(y)\cdot f(x)$.

Function Generation of Several Variables

So far it was supposed that the supply voltage U to the potentiometers Q of Fig. 1, defining the reference voltages of the amplitude comparators, was held constant. Varying this voltage, we see that new possibilities of application of the function generator arise. We shall explore the results of this modification.

Let us set

$$v(x) = \text{const.}$$

so that the circuit works as a function generator

$$e = k_1 \cdot f[k_2 \cdot g(x)]. \tag{4}$$

The scale factor k_1 depends on the constant voltage supply to the potentiometers P, and the scale factor k_2 on the voltage U supplying the potentiometers Q, as seen in Fig. 1.

In the general case, (4) can be written in the form

$$e = f(x, k_1, k_2).$$

The transformation of the parameters k_1 and k_2 into corresponding variables y and z is achieved by the well-known electronic method of scanning continuously the variable x in one minor cycle and y, z in discrete steps in a major cycle. Thus we dispose in principle with a three-variable function generator

$$e = f(x, y, z)$$

or more precisely

$$e = f(x_p, y_r, z_s)$$

where p, r, s = positive integers. In the further text the indexes p, r, s, indicating that discrete values of the desired function are generated, will be omitted.

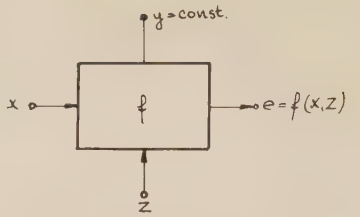

Fig. 7—Generation of $e=f(x, z)$.

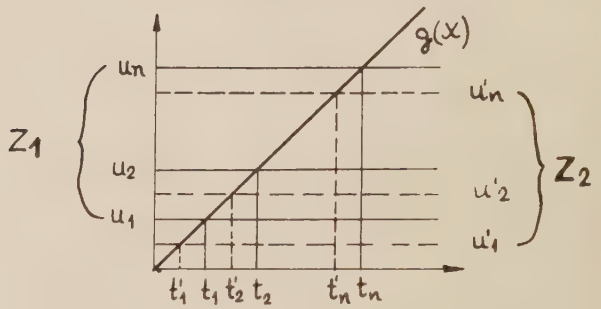

Fig. 8—Influence of variable bias voltage U on amplitude comparators.

We shall analyze here only the applications as a two-variable function generator

$$e = f(x, y) \qquad k_2 = \text{const.}$$

and

$$e = f(x, z) \qquad k_1 = \text{const.}$$

The case

$$k_2 = \text{const.},$$

i.e., the supply voltage U in Fig. 1, being held constant with the input to the potentiometers P varied in a stepwise manner, is represented by the block diagram in Fig. 5. Since the reference levels of the amplitude comparators are set in the normal linear relation, $h(n)$ is omitted in Fig. 5.

A more general form of the function generator is represented in Fig. 6 where y itself is fed through a one-variable function generator. The equation of such a function generator is evidently

$$e = f(x)\cdot v(y). \tag{5}$$

A second type of two-variable function generator is represented in Fig. 7. The supply voltage U to the potentiometers Q of Fig. 1 is now varied in a discrete manner.

The influence of this variation is best explained by using the graphical representation of Fig. 8. The reference voltages of the amplitude comparators of Fig. 1 are supposed to be set as

$$\Delta u = \text{const.}$$

The values t_n and t_n', respectively, represent the instants when switches S are closed. It is also supposed, without loss of generality, that $g(x)$ is a sawtooth waveform and

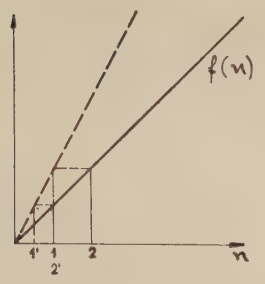

Fig. 9—Influence of variable bias voltage U on $f(n)$.

$$f(n) = n$$

s shown in Fig. 9. A decrease in the common supply oltage U of the amplitude comparators has the general ffect of shifting all the points of intersection t_n in Fig. 8 o the left. Because the electronic switches close at these istants, the same is true for the ordinates $f(n)$ stored n the potentiometers P. This is demonstrated in Fig. 9.

In mathematical terms, the variation of the supply oltage U is inversely proportional to the scale factor k_2, o that (4) now reads

$$e = f\left(\frac{x}{z}\right). \tag{6}$$

x and z are fed through one-variable function genera-ors, then

$$e = f\left[\frac{g(x)}{s(z)}\right]. \tag{7}$$

Applying these results to (3), a more general expres-on is obtained:

$$e = fh^{-1}\left[\frac{g(x)}{s(z)}\right]. \tag{8}$$

The network performing the transformation (8) is given n Fig. 10.

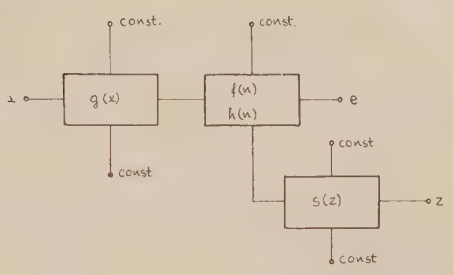

Fig. 10—Generation of (8).

Although this function generator does not solve the general problem

$$e = f(x, y)$$

in a direct form, (5) to (8) cover a large field of practical applications. This technique is directly applicable, for instance, to all types of kernel functions of the form

$$f(x \cdot y)$$
$$f(x \pm y)$$
$$f[y(x) \cdot s(y)].$$

Using approximate formulas and additional equipment, other types of functions can also be generated depending on each individual case.

Conclusion

A review of the operations performed by the network of Fig. 1 shows that it is possible to realize multi-input circuits with very general nonlinear transfer characteristics. Researches in this direction, apart from the theoretical interest, can be very helpful in designing electronic devices for analog computation. The network in question, although suitable for a variety of mathematical applications, consists only of simple and identical elements.

Synthesis of N-Valued Switching Circuits*

R. D. BERLIN†

Summary—The concept of a functionally complete set is defined and examples are given in the familiar field of 2-valued logic and 2-valued switching circuits.

Several functionally complete sets, already known to investigators in n-valued logic, are discussed, with particular emphasis on applications to the synthesis of n-valued switching circuits.

It is noted that much of the switching in a base-n computer will be, in a sense, binary, permitting the use of relatively simple elements in the synthesis. As an example, an n-valued switching matrix is synthesized.

I. Introduction

EVERY practical digital computer constructed so far has used some bistable device (vacuum tube or transistor flip-flop, magnetic core, etc.) as its basic static memory element. Since it is possible to construct devices possessing more than two stable states it is of some interest to learn whether mathematical tools can be developed (comparable to Boolean algebra for 2-valued switching) which also will lead directly to switching function synthesis.

One purpose of this paper is to point out that a preliminary choice of basic gating elements must be made before such mathematics can be developed. This choice must be based primarily on ease and economy of physical realizability, and it will not be attempted in this paper. It is hoped, however, that other people will interest themselves in the question.

In order to avoid confusion between devices composed of several bistable elements which, though possessing many stable states, must be set and sensed along several lines, and what we choose to regard as basic multistable devices, we will assume that the state of a *basic* memory element can be sensed by examining only its one output line. It thus becomes meaningful to evaluate multistable memory elements by comparing them to devices possessing an equal number of stable states, but composed of bistable elements.

II. The Concept of Functional Completeness

We mean by a (combinational) switching circuit one with a finite number of inputs: $X_1, X_2, \cdots, X_n$, and a finite number of outputs: $f_1(X_1, X_2, \cdots, X_n)$, $f_2(X_1, X_2, \cdots, X_n)$, $\cdots$, $f_m(X_1, X_2, \cdots, X_n)$, wherein the present state of each output is determined solely and uniquely by the present state of each input. By a p-valued switching circuit we will mean one wherein each input and each output always will be in one of p states; p is always finite.

We will call the functions $f_i(X_1, X_2, \cdots, X_n)$, $i=1, 2, \cdots, m$, which define each output state for every combination of input states, switching functions. The range of the X's and the domain of the f's will be the same set of p elements (values, states) so that functions always can be composed in all possible ways. For example, given $f_1(X_1, X_2)$ and $f_2(X_1, X_2)$,

$$f_3(X_1, X_2) = f_1[f_2(X_1, X_2), X_1]$$

has meaning. Physically, we require that all outputs be usable as inputs. Let the p states be denoted by $C_0, C_1, \cdots, C_{p-1}$.

We prove first that if it is possible to synthesize (compose) all functions of 2 variables for a given p, then it is already possible to synthesize all functions of any number of variables. (See Webb[1] for another form of this proof.)

Arguing by induction, we show that it is possible to synthesize a function $f(X_1, X_2, \cdots, X_n, X_{n+1})$ of $n+1$ variables if it is assumed that all functions of a fewer number of variables can be synthesized.

Our method is to employ first an induction on the subscript of $g_k(X_1, X_2, \cdots, X_n, X_{n+1})$, defined as follows:

$$g_k(X_1, X_2, \cdots, X_n, C_i) = \begin{cases} f(X_1, X_2, \cdots, X_n, C_i); & i \leq k \\ C_0; & k < i \leq p-1. \end{cases}$$

That is, given g_k, we synthesize g_{k+1}. Then we construct g_0 directly. (g_{p-1} will be f.)

The function $H_k(y_1, y_2, y_3)$, constructed so that

$$H_k(y_1, y_2, C_i) = \begin{cases} y_1; & i \leq k \\ y_2; & i = k+1 \\ C_0; & i \geq k+2, \end{cases}$$

is precisely $g_{k+1}(X_1, X_2, \cdots, X_n, X_{n+1})$ if we let $y_1 = g_k(X_1, X_2, \cdots, X_n, X_{n+1})$ and

$$y_2 = f(X_1, X_2, \cdots, X_n, C_{k+1}).$$

y_2 is constructed on the basis of our inductive assumption. This assumption does not yet guarantee the possibility of constructing H_k (for suppose $n+1=2$). We show directly a method for synthesizing a function of three variables, $R(X_1, X_2, X_3)$. Suppose we have already constructed

$$R_k(X_1, X_2, X_3) = \begin{cases} R(X_1, X_2, X_3); & X_3 = C_i, \ i \leq k \\ C_0; & X_3 = C_i, \ i > k \end{cases}$$

then

$$R_{k+1}(X_1, X_2, X_3) = G_1\{R_k(X_1, X_2, X_3), G_2[R(X_1, X_2, C_{k+1}), X_3]\}$$

* Manuscript received by the PGEC, July 25, 1957; revised manuscript received, December 30, 1957.

† General Electric Co., Syracuse, N. Y.

[1] D. L. Webb, "Generation of any n-valued logic by one binary operation," *Proc. Natl. Acad. Sci.*, vol. 21, pp. 252–254; May, 1935.

TABLE I
TWO-VALUED FUNCTIONS OF TWO 2-VALUED VARIABLES

x_1	x_2	f_0	f_1	f_2	f_3	f_4	f_5	f_6	f_7	f_8	f_9	f_{10}	f_{11}	f_{12}	f_{13}	f_{14}	f_{15}
0	0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
0	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
1	0	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

here the functions of two variables, G_1 and G_2, are defined as follows

$$G_1(y_1, C_0) = G_1(C_0, y_1) = y_1$$

$$G_2(y_1, y_2) = \begin{cases} C_0; & y_2 \neq C_{k+1} \\ y_1; & y_2 = C_{k+1}. \end{cases}$$

ut now $R_{p-1} = R$, and R_0 is easily constructed since

$$R_0(X_1, X_2, X_3) = G[R(X_1, X_2, C_0), X_3],$$

here

$$G(y_1, y_2) = \begin{cases} y_1; & y_2 = C_0 \\ C_0; & y_2 \neq C_0. \end{cases}$$

Now

$$_{p-1}(X_1, X_2, \cdots, X_n, X_{n+1}) = f(X_1, X_2, \cdots, X_n, X_{n+1}).$$

nd, since

$$(X_1, X_2, \cdots, X_n, X_{n+1}) = G[f(X_1, \cdots, X_n, C_0), X_{n+1}],$$

ne original assertion is proved.

Thus, the synthesis problem is, in theory, solved completely if a method is known for synthesizing functions f 2 variables.

The problem of synthesizing or "composing" all -valued functions of p-valued variables is one which as, in other contexts, long concerned logicians. Borowing from their terminology, we call a set of functions "functionally complete," or a "basic set," for a xed p, if the set of the functions which can be defined xplicitly from the functions of the set[2] is exactly the set f all p-valued functions. Here we will simplify our otation by denoting the p values $C_0, C_1, \cdots, C_{p-1}$ nerely by their subscripts, ascribing none of the usual rithmetic properties to the new symbols, $0, 1, \cdots, p-1$.

For $p=2$, the functionally complete sets are already amiliar to designers of 2-valued switching circuits. The ixteen distinct 2-valued functions of two 2-valued ariables are given in Table I. The identity functions $_0 \equiv X_2$ and $f_{12} \equiv X_1$, and the constant functions $f_0 \equiv 0$ nd $f_{15} \equiv 1$, can, with good practical reason, be taken as lready synthesized.

The following sets of functions are functionally complete:

1) $f_8(X_1, X_2)$ and $f_3(X_1)$ [we drop X_2 in writing $f_3(X_1, X_2)$ since

$$f(X_1, 0) = f(X_1, 1) \text{ for } X_1 = 0, \text{ or } 1],$$

2) $f_{14}(X_1, X_2)$ and $f_3(X_1)$,
3) $f_7(X_1, X_2)$.

To make the meaning clear, we prove 1) above by exhibiting the following listing, each line of which can be verified by direct substitution: (f_3, f_8, f_{10}, f_{12} are given)

$$f_{14} = f_3\{f_8[f_3, f_3(f_{10})]\} \quad (1)$$
$$f_0 = f_8(f_3, f_{12}) \quad (2)$$
$$f_1 = f_3(f_{14}) \quad (3)$$
$$f_2 = f_8(f_3, f_{10}) \quad (4)$$
$$f_4 = f_8[f_{12}, f_3(f_{10})] \quad (5)$$
$$f_5 = f_3(f_{10}) \quad (6)$$
$$f_6 = f_{14}(f_2, f_4) \quad (7)$$
$$f_7 = f_3(f_8) \quad (8)$$
$$f_9 = f_3(f_6) \quad (9)$$
$$f_{11} = f_3(f_4) \quad (10)$$
$$f_{13} = f_3(f_2) \quad (11)$$
$$f_{15} = f_{14}(f_3, f_{12}). \quad (12)$$

We give one example (Fig. 1), using (1) above, to illustrate the familiar method of translating functional compositions into logical block diagrams.

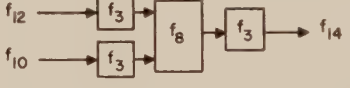

Fig. 1—Logical block diagram.

The functions $f_8(X_1, X_2)$ and $f_3(X_1)$ are commonly referred to as "X_1 and X_2" and "not X_1," respectively. Frequently the binary connective "$\cdot$" and the unary operator "$'$" are used in place of the above functional notation: $f_8(X_1, X_2) = X_1 \cdot X_2$ and $f_3(X_1) = X'$. $f_8(X_1, X_2)$ and $X_1 \cdot X_2$ can refer to a complete description of the function, or can be used to designate the image of the couple (X_1, X_2) under the mapping, depending upon the context. This is also true for $f_3(X_1)$ and X_1'.

Equally familiar is the functionally complete set consisting of f_3 and f_{14}. The latter is commonly referred to as "X_1 or X_2," and is written "$X_1 + X_2$."

Since both f_8 and f_{14} are physically realizable at roughly equal costs, it is common practice to economize by employing both as elementary "blocks."

[2] We will consider fundamentally complete sets always to include he identity functions without specifically mentioning them.

It is worth noting that f_7, commonly referred to as the "Sheffer stroke function," written X_1/X_2, alone forms a functionally complete set.[3] Two basic reasons that this function is not employed as an elementary block are: 1) it has not been possible to construct such an element except as a superstructure of f_3, f_8, and f_{14}'s; 2) even if a basic block realizing this element were to cost no more than an f_8 or f_{14} block, exclusive use of this block would, in general, increase the cost of synthesis. (Merely adding f_7 to f_3, f_8, and f_{14} would clearly reduce the cost.)

III. Examples of Functional Completeness

A. Post, in 1921,[4] demonstrated that for any p the two functions described in Table II are sufficient to synthesize all functions of 2 variables (and hence, by our last argument, functions of any number of variables).

If the elements are ordered by their labels in the usual arithmetic sense, then it is clear that f_1 merely maps each element into the element immediately following it (with the added convention that $p-1$ maps into 0, closing the cycle), and that f_2 maps i, j into whichever of i and j is "larger."

TABLE II
Post's Functions

x	$f_1(x)$	x_1x_2	$f_2(x_1, x_2)$
0	1	0 0	0
1	2		
·	·	—	
·	·		
·	·	i_1 j_1	i_1 for $i_1 \geq j_1$
$p-1$	0	—	
		i_2 j_2	j_2 for $i_2 \leq j_2$
		—	
		$p-1, p-1$	$p-1$

The physical realization of these functions is easily conceived. For example, if $p-1, p-2, \cdots, 1$ and 0 are taken to be distinct voltage levels $e_{p-1}, e_{p-2}, \cdots, e_1$, and e_0, with $e_i > e_j$ for $i < j$, then f_2 is realized by any device which passes the higher of two voltage levels on its inputs.

A severe drawback of the above set of basic functions (which appears to apply to any set which is economical in the sense of containing not more functions than are essential) is that any canonical form of a function in terms of these basic functions will be long and complicated, and, in unreduced form, costly to realize.

Note: We will say that a functional form is canonical with respect to a given basic set of functions if:

1) The form is obtained by composition of constants, variables, and functions of the basic set,
2) Every function can be expressed in such form,
3) Distinct forms represent distinct functions (two functions are distinct if they differ in any "truth table" entry).

[3] H. M. Sheffer, "A set of five independent postulates for Boolean algebra with application to logical constants," *Trans. Amer. Math. Soc.*, vol. 14, pp. 481–488; 1913.

[4] E. L. Post, "Introduction to a general theory of elementary propositions," *Amer. J. Math.*, vol. 43, pp. 163–185; 1921.

Thus

$$f(X_1, X_2) = \overline{a_{00} + X_1 + X_2} + \overline{a_{01} + X_1 + \overline{X}_2} + \overline{a_{10} + \overline{X}_1 + X_2} + \overline{a_{11} + \overline{X}_1 + \overline{X}_2}$$

where

$$a_{ij} = \overline{f(i, j)}$$

is a canonical form for 2-valued functions of two 2-valued variables with respect to the basic set consisting of the familiar unary function, "not X," and the binary function, "X or y."

B. A functionally complete set (similar to that of Post) may be so derived that a detailed synthesis procedure is already indicated. Take, for example, for $p=3$, the two functions described in Table III, which we show to comprise such a set.

TABLE III
The Functions $P_1(X, y)$ and $P_2(X, y)$

X	y	$P_1(X, y)$	X	y	$P_2(X, y)$
0	0	0	0	0	0
0	1	1	0	1	0
0	2	2	0	2	0
1	0	1	1	0	0
1	1	2	1	1	1
1	2	0	1	2	2
2	0	2	2	0	0
2	1	0	2	1	2
2	2	1	2	2	2

Suppose that $P(X, y)$ is to be synthesized using P_1 and P_2. It is easily shown[5] that the system of nine equations

$$P(i, j) = A_{00} + A_{01}i + A_{02}i^2 + A_{10}j + A_{11}ij + A_{12}i^2j + A_{20}j^2 + A_{21}ij^2 + A_{22}i^2j^2$$
$$i = 0, 1, 2; \; j = 0, 1, 2$$

can be solved, modulo 3, for the nine coefficients A_{mn}, $m, n = 0, 1, 2$; that is, the polynomial $\sum_{m,n} A_{mn}X^n y^m$ passes through the required nine points $[(i, j), P(i, j)]$ and thus represents the function $P(X, y)$. Since the polynomial is constructed only by combining constants and variables under addition and multiplication (P_1 and P_2), it is clear that P can be synthesized, and that the above polynomial form describes the process in detail.

The above method can be extended easily to any prime p, and, with a few refinements, to any p whatever.

A conspicuous advantage, gained by the use of gates which realize the functions P_1 and P_2, is that the elements 0, 1, and 2 (for the general case, the elements $0, 1, \cdots, p-1$, p a prime, where P_1 and P_2 are addition

[5] D. Tamari, "Some mutual applications of logic and mathematics," *Proc. Second International Colloquium of Mathematical Logic*, pp. 89–90; August, 1952.

l multiplication, mod p, respectively) form a "field"[6] h respect to these operations. In short, all the fa- iar arithmetic rules employed in the field of real mbers apply here. Furthermore, nearly all the theo- ns of matrix algebra are valid over arbitrary fields. us the answers to switching problems, particularly the little known area of sequential switching, could looked for in the vast literature of this field. (Inter- ing results in the area of 2-valued sequential switch- have been obtained by Huffman[7] and others by pping the "or" gate as a synthesizing element and ng a modulo-2 adder plus the conventional "and" or mes" gate as basic functions. These are the P_1 and P_2 ve, and thus the elements 0 and 1 form a field.)

C. Webb[1] demonstrated that the following function ne forms a functionally complete set

$$W(X, y) = \begin{cases} 0; & X \neq y \\ X + 1 \pmod{p}; & X = y. \end{cases}$$

may be conjectured from the method by which the mpleteness is proved, that the canonical form would exceedingly lengthy and complex.

Examples can readily be given to demonstrate the nplicity of canonical forms which can be obtained by mplicating the functions of the basic set. A recent per,[8] in which 3-valued functions are synthesized, de- ops a basic set consisting solely of the function $X_1, X_2, X_3, X_4)$, there referred to as a T gate, which lefined by

$$T(X_1, X_2, X_3, X_4) = \begin{cases} X_1; & X_4 = 0 \\ X_2; & X_4 = 1 \\ X_3; & X_4 = 2. \end{cases}$$

s easily checked by recognizing that T will be X_1, X_2, X_3, depending on whether X_4 is 0, 1, or 2, respectively, at

$$f(X_1, X_2) = T\{f(0, X_2), f(1, X_2), f(2, X_2), X_1\}$$

any f. The $f(0, X_2)$, $f(1, X_2)$, and $f(2, X_2)$, each a action of a single variable, are easily obtained from

$$f(X) = T\{f(0), f(1), f(2), X\}.$$

bstituting this in the expression for $f(X_1, X_2)$ above, relatively simple canonical form results. Note that power, and at the same time the complexity, of the function are a consequence of making 4 inputs avail- le. This requires that distinctions be made among = 81 different input conditions compared to 9 or 3 for ary or unary basic functions.

Indeed, a function, $F(z_0, z_1, \cdots, z_{p^n-1}, w_1, \cdots, w_n)$, of p^n+n variables can always be defined which alone will serve as a basic set for all p-valued functions of p-valued variables, and with respect to which the canonical form is simply F, with the variable spaces appropriately filled.

More precisely, let

$$F(z_0, z_1, \cdots, z_{p^n-1}, w_1, \cdots, w_n) = z_{\{w_1 w_2 \cdots w_n\}}$$

where $\{w_1 w_2 \cdots w_n\}$ signifies the decimal equivalent of the p-ary number $w_1 w_2 \cdots w_n$. Then, clearly

$$f(X_1, X_2, \cdots, X_n) = F[f(0, 0, \cdots, 0), f(0, 0, \cdots, 0, 1), \cdots, f(p-1, p-1, \cdots, p-1), X_1, \cdots, X_n].$$

IV. A p-Valued Switching Matrix

A computer can be conceived in which multistable (say p-state) memory elements are employed, each to represent a digit of a p-ary number. Now, outside of the arithmetic unit, much of the switching will consist of routing or gating p-ary information with p-ary control words through gates which are either open or closed. That is, many of the gating functions will be of the form $f(X, y)$, where

$$f(0, y) = 0$$
$$f(1, y) = y,$$

and the range of X is restricted to 0 and 1.

Generalizing this view, we can see the need for an n-input, p^n-output, matrix wherein one and only one of the outputs is 1, the remainder 0, and these outputs activating gates of the type indicated above.

Using a notation of Webb,[1] we introduce the special function $R_{ij}(X, y)(i=0, 1, \cdots, p-1; j=0, 1, \cdots, p^2-1)$, defined as that function which takes the value i on $X=k$, $y=h$, where $\{kh\}=j$ ($\{kh\}$ denotes the decimal equivalent of the two-digit p-ary number: kh); and the value 0 elsewhere. For example, for $p=3$, $R_{2,6}$ would be given by Table IV.

TABLE IV
THE FUNCTION $R_{2,6}$

X	y	$R_{2,6}(X, y)$
0	0	0
0	1	0
0	2	0
1	0	0
1	1	0
1	2	0
2	0	2
2	1	0
2	2	0

We will use these functions to synthesize the above switching matrix.

We note in passing that if the R_{ij}'s are available over the entire range of i and j, then these, plus Post's second function, f_2, already comprise a basic set. (It will be recalled that $f_2(0, y)=f_2(y, 0)=y$.) Suppose a function,

[6] G. Birkhoff and S. Maclane, "A Survey of Modern Algebra," e Macmillan Co., New York, N. Y.; 1948.
[7] D. A. Huffman, "The synthesis of linear sequential coding net- ks," paper presented at the Third London Symposium of In- mation Theory, London, England, September 13, 1955.
[8] C. Y. Lee and W. H. Chen, "Several valued combinational tching circuits," *Commun. and Electronics*, no. 25, pp. 278–283; y, 1956.

$g(X, y)$, is to be composed. Using the collection $R_g(k, h)$, $\{k, h\}$ in a manner symbolized in block diagram form in Fig. 2, the "outputs," of which no more than one is nonzero, can be compounded by use of the Post function as shown in Fig. 3. It will be recalled that f_2, the general "or" function, is easily realized, at least in terms of voltage levels.

The above demonstration of the functional completeness of f_2 plus the R_{ij} functions permits the conclusion that, in particular, the switching matrix which we have set out to synthesize could be constructed in a straightforward manner using this set. However, an R_{ij} is not, in general, easy to construct. Taking advantage of the binary character of the outputs, and the fact that one and only one output is nonzero over all inputs, the R_{ij}'s required can be made relatively few and simple.

The first bank of logical elements will consist of p^2 functions defined as follows:

$$S_{ij}(X, y) = \begin{cases} 0; & X = i, \ y = j \\ \neq 0; & \text{otherwise.} \end{cases}$$

The S's will range over all p^2 values of the couple (i, j). Each element will have the same two inputs denoted X_1 and X_2.

The second bank will consist of p^3 of the functions $S_{k,0}$. Each of the p^2 outputs of the first bank of S_{ij}'s serves as a y input to a set of pS_{k0}'s, where k ranges from 0 to $(p-1)$. The X input is common to all p^3 $S_{k,0}$'s, and is denoted by X_3.

In general, the mth bank $(m=2, 3, \cdots, n-1)$ will consist of p^{m+1} of the functions $S_{k,0}$. Each of the p^m outputs of the $(m-1)$th bank serves as a y input to a set of p $S_{k,0}$'s, where k ranges from 0 to $(p-1)$. The X input is common to all p^{m+1} $S_{k,0}$'s, and is denoted by X_{m+1}.

Note that the S_{ij} function is much less restrictively defined than an R function, since any one of $p-1$ outputs is permitted for all but one of the p^2 possible inputs. $S_{k,0}$ is even simpler: any value other than 0 on the y input serves to inhibit a 0 output.

V. Conclusion

We have given examples to illustrate the following possible choices of functions (or "gates") for the basic set:

1) It can consist of only one function, with respect to which the canonical form is simple. The function, however, will be extremely complex. Examples were the T gate, and the function F, discussed in Section III-C.

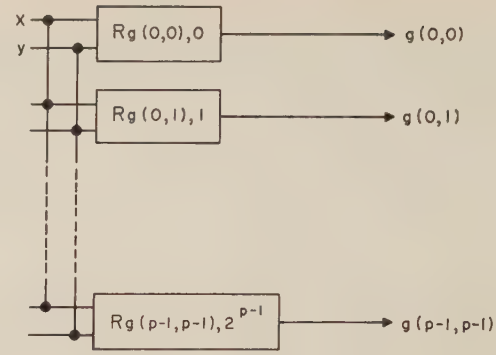

Fig. 2—The composition of $g(i, j)$; i, j, fixed.

Fig. 3—The composition of $g(X, y)$.

2) It can consist of simple functions with respect to which the canonical form is simple. The number of distinct functions required, however, will be large. An example was the set of R_{ij} functions along with Post's f_2 function. (We say that the functions are simple in this sense only: they will be functions of no more than two variables.)

3) It can consist of a single function of only two variables. The canonical form, however, will be exceedingly complex. An example was the function of Webb (see Section III-C). Another way of phrasing this last difficulty is to say that a given function can be synthesized from such a basic set in a completely predetermined manner only by initially selecting a configuration employing an excessive number of gates. We leave moot the question of how far and how easily such a configuration could then be simplified.

In the search for a workable basic set, each of the above extremes must be avoided.

It should be noted that while most of the basic sets discussed here were minimal in the sense that the removal of any one would destroy functional completeness, this type of elegance can readily be discarded in favor of a redundant, but more workable, set. In two-valued synthesis, for example, while either "or" gates or "and" gates plus inverting gates are sufficient, it is universal practice to employ all three.

Synthesis of Electronic Circuits for Symmetric Functions*

GEORGE EPSTEIN†

Summary—This paper develops a systematic method for the synsis of electronic circuits which must realize symmetric Boolean ctions. The "fold-down" method, originated by Shannon [1], ves the problem nicely for relay circuits. The electronic circuit, wever, composed of "and," "or," and "not" elements, does not m to incorporate the feature of symmetry as readily.

It is shown that for symmetric functions a minimal-not condition sts, and that this form is a powerful tool for synthesis. The nimality is not actually proven, except for the case of fundamental nmetric functions. As with the minimal-or circuit, a minimal-not cuit does not necessarily imply the most economical realization, l the design procedure should take account of this fact.

Introduction

We introduce below the simple symmetric functions. It will be noted that these are similar to the elementary symmetric functions of a ring in at the ring operations of $+$ and $\cdot$ are replaced by the tice operations of $\vee$ and $\wedge$, respectively. So there ll be no confusion, we state at the outset that the rd "sum" refers to the $+$ operation (sometimes called xclusive or," or "symmetric difference") and that the rd "union" refers to the $\vee$ operation. Thus $a \vee b$ is d "a or b" and is called the union of a and b, while ab read "a and b" and is called the product of a and b. he complement of a will be denoted by $\bar{a}$.

We will be concerned with Boolean algebras of n riables x_i, $i=1, 2, \cdots, n$. An atom of such a Boolean gebra is a product of the n variables x_i, $i=1, 2, \cdots, n$, here each x_i may either be complemented or not. Thus ere are 2^n atoms. Any Boolean function can be exessed as the union of atoms, and such a representation called a canonical expansion [2].

Theory

The fundamental symmetric functions of the x_i's are fined to be

$$= \bar{x}_1\bar{x}_2 \cdots \bar{x}_n$$

$$= x_1\bar{x}_2 \cdots \bar{x}_n \vee \bar{x}_1x_2\bar{x}_3 \cdots x_n \vee \cdots \vee \bar{x}_1\bar{x}_2 \cdots \bar{x}_{n-1}x_n \vee \cdots$$

$$= x_1x_2 \cdots x_n.$$

ach ρ_i is the union of all possible atoms with exactly i nbarred x's. We state without proof two basic theoms on fundamental symmetric functions [3].

Theorem 1

If a canonical expansion of a symmetric function contains an atom of ρ_i, then it contains ρ_i.

Theorem 2

Any symmetric function is a union of fundamental symmetric functions.

We follow Shannon in denoting any symmetric function by the symbol $S_{a_1a_2\cdots a_m}$, where a numbers are the subscripts of the ρ's which appear when the function is expressed as a union of fundamental symmetric functions.

The simple symmetric functions are defined to be

$$\tau_0 = 1$$

$$\tau_1 = x_1 \vee x_2 \vee \cdots \vee x_n$$

$$\tau_2 = x_1x_2 \vee x_1x_3 \vee \cdots \vee x_{n-1}x_n$$

$$\tau_3 = x_1x_2x_3 \vee x_1x_2x_4 \vee \cdots \vee x_{n-2}x_{n-1}x_n$$

$$\cdots\cdots\cdots$$

$$\tau_n = x_1x_2 \cdots x_n.$$

$$\tau_{n+1} = 0.$$

It should be noted that $\tau_j \supset \tau_{j+1}$ for $j=0, 1, \cdots, n$. This fact makes it easy to form $\tau_i \vee \tau_j$ and $\tau_i\tau_j$, and we see that the result is either τ_i or τ_j, depending on which of i and j is larger.

It is possible to express the τ's in term of the ρ's since the τ's are symmetric functions, but a more useful approach is obtained by the following theorem.

Theorem 3

$$\rho_i = \tau_i\bar{\tau}_{i+1}.$$

Proof: The right-hand side is obviously a symmetric function, and so must be a union of ρ's by Theorem 2. It is a product of terms, the first being τ_i, and the succeeding terms each being a different union of the $\bar{x}$'s taken $i+1$ at a time. Thus the right-hand side, when expanded, must be a canonical expansion which could not have an atom with less than, or more than, i unbarred x's. It does, in fact, have an atom with i unbarred x's, and so must be ρ_i, by Theorem 1.

Corollary: $\rho_i = \tau_i + \tau_{i+1}$. This follows from $\tau_i \supset \tau_{i+1}$, which implies that $\tau_{i+1}\bar{\tau}_i = 0$, so that $\rho_i = \tau_i\bar{\tau}_{i+1} \vee \bar{\tau}_i\tau_{i+1} = \tau_i + \tau_{i+1}$.

Theorem 4

Any symmetric function is a sum of simple symmetric functions.

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Proof: Since the fundamental symmetric functions are disjoint ($\rho_i\rho_j=0$ for $i\neq j$), we could restate Theorem 2 to say that any symmetric function is the sum of fundamental symmetric functions [this follows from the fact that if $ab=0$, $a\vee b=\bar{a}\bar{b}(a\vee b)=a\bar{b}\vee\bar{a}b=a+b$]. The corollary to Theorem 3 tells us that each fundamental symmetric function is a sum of simple symmetric functions, and hence any symmetric function is the sum of simple symmetric functions.

Theorem 5

$$\bigvee_{i=r}^{t}\rho_i=\tau_r\bar{\tau}_{t+1},\qquad t>r.$$

Proof: Using the facts that $x+x=0$ and $\tau_i\supset\tau_j$ if $j>i$ so that $\bar{\tau}_r\tau_{t+1}=0$, it follows that

$$\bigvee_{i=r}^{t}\rho_i=\sum_{i=r}^{t}\rho_i=\sum_{i=r}^{t}\tau_i+\tau_{i+1}=\tau_r+\tau_{t+1}$$
$$=\tau_r\bar{\tau}_{t+1}\vee\bar{\tau}_r\tau_{t+1}=\tau_r\bar{\tau}_{t+1}.$$

Theorem 6

$$x_1+x_2+x_3+\cdots+x_n=\tau_1+\tau_2+\tau_3+\cdots+\tau_n.$$

Proof: Grouping the terms on the right-hand side in pairs and using the corollary to Theorem 3, the right-hand side becomes $\rho_1+\rho_3+\rho_5+\cdots+\rho_m$, where $m=n$ if n is odd, and $m=n-1$ if n is even. Since distinct ρ_i are disjoint, the right-hand side becomes, finally

$$\rho_1\vee\rho_3\vee\cdots\vee\rho_m.$$

We now show, by induction, that the left-hand side is the union of all possible atoms with an odd number of unbarred terms. Since the left member is a symmetric function, if we can show that one atom of a ρ_i is present, we will know that ρ_i itself must be present by Theorem 1. When $n=1$, we have $\rho_1=x_1$. If the statement is true for $n=k$, consider $(x_1+x_2+\cdots+x_k+x_{k+1})=(x_1+x_2\cdots x_k)\,\bar{x}_{k+1}\vee(\overline{x_1+x_2+\cdots+x_k})x_{k+1}$. The left part of the union, multiplied out, is a function of $k+1$ variables and is, by the induction hypothesis, a union of atoms with an odd number of unbarred terms. The complemented term in the right part of this union is the union of all possible atoms in the variables $x_1,x_2,\cdots,x_k$ with an even number of unbarred terms, since the complement of a symmetric function is the union of the fundamental symmetric functions which did not appear in the original function. Multiplying this by x_{k+1} gives atoms with an odd number of unbarred terms in $k+1$ variables. It is seen that there is at least one atom present in this complete expansion which is also in a ρ_r, where r is any odd number less than or equal to $k+1$, and so we have this expression equal to $\rho_1\vee\rho_3\vee\cdots\vee\rho_m$ exactly.

Corollary:

$$1+x_1+x_2+\cdots+x_n=\tau_0+\tau_1+\tau_2+\tau_3+\cdots+\tau_n.$$

Design

It is possible, now, to write the minimal-not form for a fundamental symmetric function. Theorem 3 states that a fundamental symmetric function can always be realized with only one "not" element.

We illustrate with two examples.

Example 1

$$y=x_1\bar{x}_2\vee\bar{x}_1x_2.$$

The minimal form for this familiar function is well known. We have, in fact, using the above theory,

$$y=\rho_1=\tau_1\bar{\tau}_2=(x_1\vee x_2)(\overline{x_1x_2}).$$

Example 2

$$y=x_1\bar{x}_2\bar{x}_3\vee\bar{x}_1x_2\bar{x}_3\vee\bar{x}_1\bar{x}_2x_3.$$

Normal design techniques applied to this function would probably result in a circuit with 14 arrows. Applying Theorem 3, however, we obtain

$$y=(x_1\vee x_2\vee x_3)(\overline{x_1x_2\vee x_1x_3\vee x_2x_3})$$
$$=(x_1\vee x_2\vee x_3)[\overline{x_1x_2\vee x_3(x_1\vee x_2)}]$$

whose circuit given in Fig. 1 has 13 arrows.

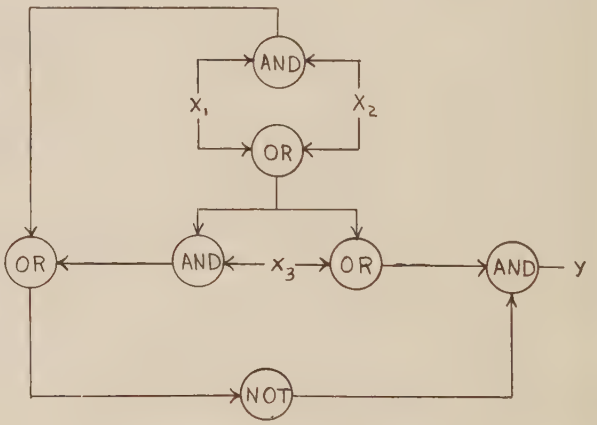

Fig. 1—Circuit with 13 arrows.

This circuit has the added feature of having no more than two inputs to any one element.

Theorem 7

One can design an electronic circuit for a symmetric function with as many "not" elements as there are subsets of consecutive numbers among the a numbers for that function.

Proof: This follows immediately from Theorem 5.

Example 3

If we have a symmetric function in 12 variables given by $S_{3\ 4\ 5\ 8\ 9\ 11}$, this function is realized by the expression $\tau_3\bar{\tau}_6\vee\tau_8\bar{\tau}_{10}\vee\tau_{11}\bar{\tau}_{12}$, which requires 3 "not" elements, the number of subsets of consecutive a numbers.

Theorem 8

The number of "not" elements required for a symmetric function in n variables does not exceed $n/2$.

Proof: This follows easily from Theorem 7. The only concern is that the number might be $(n+1)/2$. We have, using Theorem 4 and the definition of τ_{n+1},

$$\bigvee_{i=r}^{n} \rho_i = \tau_r \bar{\tau}_{n+1} = \tau_r \bar{0} = \tau_r.$$

This does not require a "not" element, and so $(n+1)/2$ is too large.

The electronic circuit obtained from Theorem 7 will be called the minimal-not circuit, although minimality is not proved in this paper. Such a circuit, however, as with the minimal-or circuit, does not necessarily imply the most economical realization. A graphic illustration of this fact is given as follows.

Example 4

$$y = x_1\bar{x}_2\bar{x}_3 \vee \bar{x}_1x_2\bar{x}_3 \vee \bar{x}_1\bar{x}_2x_3 \vee x_1x_2x_3$$
$$y = \rho_1 \vee \rho_3$$
$$= \tau_1\bar{\tau}_2 \vee \tau_3$$
$$= (x_1 \vee x_2 \vee x_3)(\overline{x_1x_2} \vee \overline{x_1x_3} \vee \overline{x_2x_3}) \vee x_1x_2x_3$$
$$= (x_1 \vee x_2 \vee x_3)(\overline{x_1x_2} \vee \overline{x_3x_1} \vee \overline{x_2}) \vee x_1x_2x_3.$$

This circuit requires 17 arrows and is shown in Fig. 2.

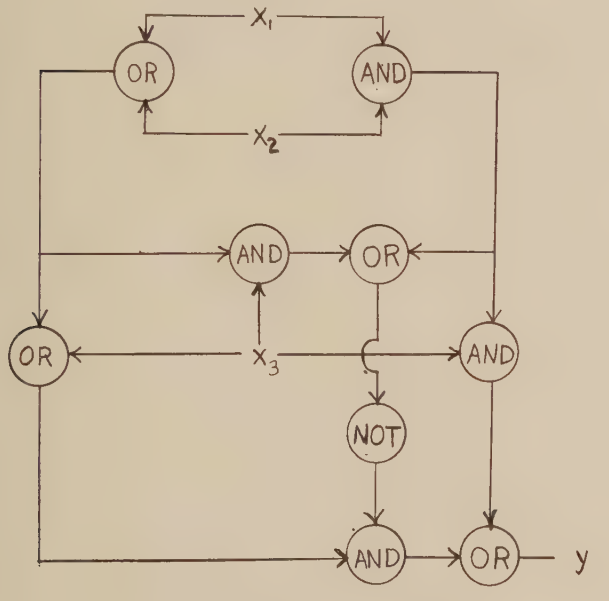

Fig. 2—Circuit with 17 arrows.

In this particular case, however, Theorem 6 is applicable. Theorem 4 says that we can write y as the sum of simple symmetric functions. We have

$$y = \rho_1 \vee \rho_3 = \tau_1 + \tau_2 + \tau_3.$$

Thus we have $y=\tau_1+\tau_2+\tau_3=x_1+x_2+x_3$ by Theorem 6, and this is the familiar function of binary adders.

Using Example 1, we have

$$y = (x_1 + x_2) + x_3 = [(x_1 \vee x_2)\overline{x_1x_2}] + x_3$$
$$= [(x_1 \vee x_2)\overline{x_1x_2} \vee x_3]\overline{(x_1 \vee x_2)\overline{x_1x_2}x_3}.$$

The circuit requires two "not" elements, but only 14 arrows, and is shown in Fig. 3.

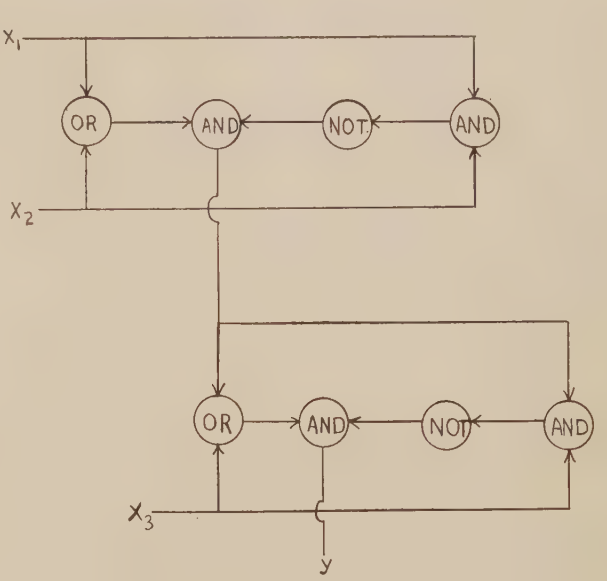

Fig. 3—Circuit with 14 arrows.

This result is easily extended to n variables. $y=x_1+x_2$ requires 7 arrows. Hence $\tau_1+\tau_2+\cdots+\tau_n=x_1+x_2+\cdots+x_n$ requires $7(n-1)$ arrows. We also have $\tau_0+\tau_1+\cdots+\tau_n=1+x_1+x_2+\cdots+x_n$, which requires $7n-6$ arrows.

We can conclude, from the last example, that a minimal-not circuit does not guarantee the best circuit. One can alternatively try to construct the circuit out of symmetric functions in fewer variables, and then compare with the minimal-not circuit to determine the better result. In the last example, $y=\tau_1+\tau_2+\tau_3$ was realized by considering it as a symmetric function in the variables (x_1+x_2) and (x_3). The procedure yielded a circuit which bettered the minimal-not circuit by 3 arrows and, perhaps more importantly, yielded a circuit consisting of two identical components.

We end with one last example.

Example 5

Design an electronic circuit which realizes the function

$$y = x_1x_2x_3x_4 \vee x_1\bar{x}_2\bar{x}_3\bar{x}_4 \vee \bar{x}_1x_2\bar{x}_3\bar{x}_4 \vee \bar{x}_1\bar{x}_2x_3\bar{x}_4 \vee \bar{x}_1\bar{x}_2\bar{x}_3x_4.$$

We see that this is $y=\tau_1+\tau_2+\tau_4$. τ_3 is absent so we cannot use Theorem 6.

We have

$$y=\rho_1\vee\rho_4=\tau_1\bar{\tau}_2\vee\tau_4$$
$$=(x_1\vee x_2\vee x_3\vee x_4)(\overline{x_1x_2\vee x_1x_3\vee x_1x_4\vee x_2x_3\vee x_2x_4\vee x_3x_4})$$
$$\vee x_1x_2x_3x_4$$
$$=[(x_1\vee x_2)\vee(x_3\vee x_4)][\overline{x_1x_2\vee(x_1\vee x_2)(x_3\vee x_4)\vee x_3x_4}]$$
$$\vee(x_1x_2)(x_3x_4).$$

The circuit in Fig. 4 has 22 arrows. This circuit, obtained through the above theorems, is the simplest the author has been able to find. One other attempt is to use symmetric functions in the three variables x_1, x_2, and x_3, to realize the function:

$$y = x_4(\bar{x}_1\bar{x}_2\bar{x}_3\vee x_1x_2x_3)\vee\bar{x}_4(\bar{x}_1\bar{x}_2x_3\vee\bar{x}_1x_2\bar{x}_3\vee x_1\bar{x}_2\bar{x}_3)$$
$$y = x_4[\overline{(x_1\vee x_2\vee x_3)}\vee x_1x_2x_3]$$
$$\vee\bar{x}_4(x_1\vee x_2\vee x_3)(\overline{x_1x_2\vee x_1x_3\vee x_2x_3})$$
$$y = x_4[\overline{(x_1\vee x_2\vee x_3)\vee x_1x_2x_3}]$$
$$\vee[\overline{x_4\vee\overline{x_1x_2}\vee\overline{x_3(x_1\vee x_2)}}](x_1\vee x_2\vee x_3).$$

This circuit, however, requires 23 arrows.

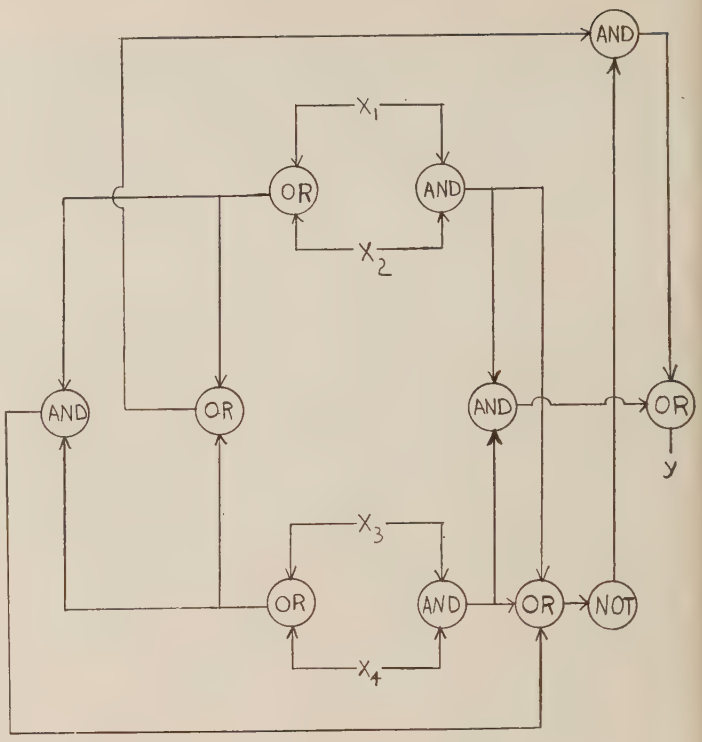

Fig. 4—Circuit with 22 arrows.

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Correction

F. P. Brooks, Jr., *et al.*, authors of "An Experiment in Musical Composition," which appeared on pages 175–182 of the September, 1957 issue of these Transactions have brought the following correction to the attention of the editor.

On page 179, line 5, 1.3 μsec should read 1.3 msec.

Thermistors for the Gradual Application of Heater Voltage to Thermionic Tubes*

J. J. GANO† AND G. F. SANDY†

Summary—Thermistors which are thermally-sensitive resistors having large negative temperature coefficients of resistance can be optly used for the gradual application of heater voltage to thermionic tubes, thereby diminishing thermal transients and reducing mechanical failures. Full voltage is first applied to the thermistor and load in series and after temperature equilibrium is reached, the thermistors are shorted out. From a cold start thermistor resistance decreases by a factor of approximately 100 and heater resistance increases by a factor of 5 to 10. By selecting a set of series-connected thermistors to limit the current to a maximum of 120 per cent of the operating value during the voltage application, the initial voltage on the heaters will be less than 5 per cent of rated, and the voltage before shorting out, about 75 per cent of rated. Peak currents occur twice, once while the thermistors are in the circuit and again when the thermistors are shorted out at 90 seconds. One set of thermistors can be used to limit the current satisfactorily over a wide range of loads. The most favorable number of thermistors to connect in series is determined experimentally. Commercially available units in washer form can accommodate heater loads up to 1100 watts.

Introduction

IN LARGE electronic systems, such as those employing large scale digital computers where the tube-count can run to tens of thousands, long tube life is a necessity. To extend tube life, one precaution that should be taken is the prevention of thermal shocks to the filaments caused by the large inrush currents upon the sudden application of power. Welds that secure the filament to the base pins become overheated and are likely to break after repeated stressing. In tubes where the filament is placed within the cathode sleeve, the filament wires lengthen rapidly and rub against the cathode, removing insulation from the filament wires and resulting in cathode-to-heater shorts. Sharp bends in folded filaments also develop stresses which cause open circuits.

Ideally, thermal shock would be minimized by the uniform acceleration and deceleration of the filament temperature to its operating value. Because such a scheme is impractical, many different methods are used to reduce the thermal effects. In some systems the filaments are continuously energized except for long-duration shutdowns. At the other extreme, elaborate devices gradually increase the voltage to the filaments when power is first applied. These devices are usually incorporated into the regulators which control the filament voltage for the entire system.

Large electronic systems, however, are generally subdivided into smaller logical sections which are packaged separately. The separate application and removal of power to the individual sections facilitates trouble shooting and minimizes the number of times the entire system is energized and de-energized. In such large installations, power is applied and removed more often from any given section by local control than by the control which operates the entire power system. Consequently, filament voltage is usually applied at the section level rather than at the systems level. For this purpose, thermistors, which are resistors having negative temperature coefficients of resistance, may be applied to give gradual filament heating.

Thermistors have been used in time delay applications, temperature measurements, and amplifier stabilizing circuits. At least one manufacturer has used them in series heater strings for television receivers. All of these are low current applications. This paper will discuss the use of thermistors to control more than one kilowatt of power. A physical description of typical commercially available thermistors and recommended mounting methods are presented in the Appendix.

Performance of Thermistors

Thermistor current ratings make them suitable for connection in the primary side of the transformers as shown in Fig. 1. The voltage is initially applied to the filaments with the thermistors in series by closing Contact A. The voltage across the filaments increases slowly and after an equilibrium voltage is reached the thermistor is shorted out by closure of Contact B. The fact that power is removed from the filaments abruptly is not as serious as sudden application because cooling of the filaments is due primarily to radiation, a slow process. To obtain a gradual increase of voltage, the thermal response of the thermistors must be much slower than that of the filaments. Otherwise the thermistor resistance decreases rapidly, and the filament voltage and current increase too rapidly. Fig. 2 shows a typical response of filament current when full voltage is applied directly to a filament load. The final current is reached in a few seconds. By applying thermistors which have a thermal response several times slower, the voltage across the filaments can be gradually increased. The thermal response is dependent on the heat capacity and the radiation properties of the thermistor.

Effect of Number of Thermistors in Series

From a cold start to the time of shorting, thermistor resistance decreases by a factor of approximately 100 and heater resistance increases by a factor of 5 to 10.

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† Lincoln Laboratory, M.I.T., Lexington, Mass.

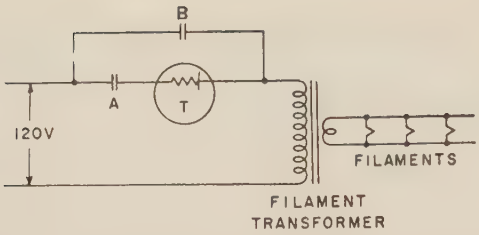

Fig. 1—Circuit for gradual application of voltage to filaments.

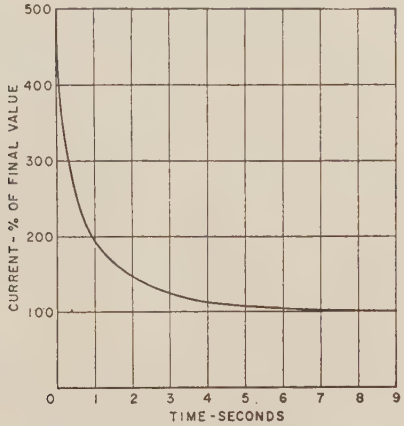

Fig. 2—Current response upon application of full voltage to a filament load.

Both of these characteristics are helpful. Because commercially available thermistors having current ratings above $\frac{1}{2}$ do not have sufficient thermal capacity to obtain the slow thermal response required, they cannot be applied singly in series with the load. By electrically connecting a number of thermistors in series, the thermal capacity is increased without sacrificing the necessary current rating. The effect of varying the number of thermistors in series for a fixed filament load is shown in Fig. 3. For a particular curve, a peak of current occurs while the thermistors are in the circuit and another peak occurs when the thermistors are shorted out at 90 seconds. The tubes are ready to operate after two minutes. The first peak is caused by the rapid decrease in the thermistor resistance. As the number of thermistors is increased, the magnitude of the first peak is reduced and occurs at a later time. The magnitude of the second peak increases because of the lower voltage across the filaments before shorting of the thermistors. The most favorable number of thermistors is that which makes the two peaks equal. Any further increase in the number reduces the first peak but increases the second. By selecting the proper number of thermistors, the maximum current at any time during the gradual voltage increase and during shorting is limited to less than 120 per cent of the final value. The initial voltage on the filaments is less than 5 per cent of rated, and the voltage before shorting is about 75 per cent of rated.

Effect of Filament Load

The curves of Fig. 4 show that one set of thermistors can be used to limit the filament current satisfactorily for a wide range of loads. Two factors determine the

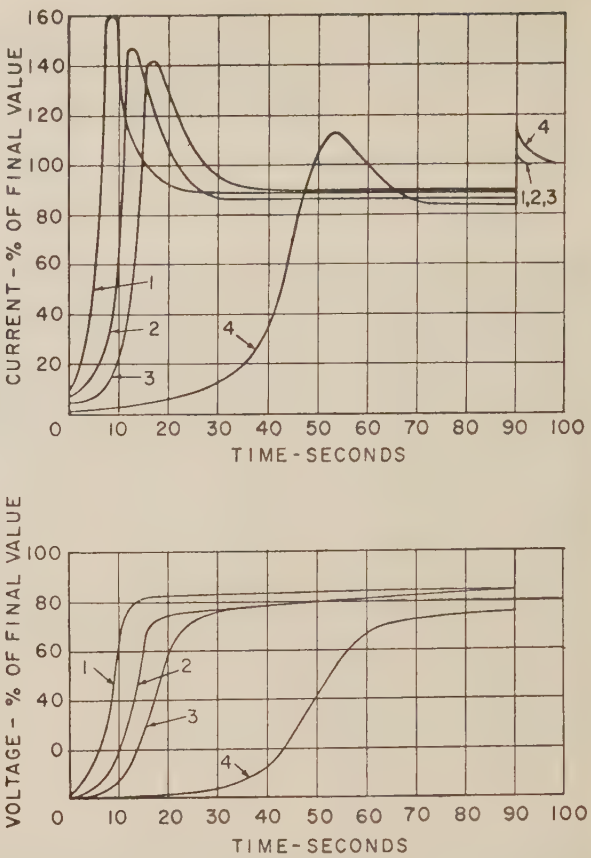

Fig. 3—Filament voltage application. Effect of number of thermistors in series, 1) 6 in series, 2) 8 in series, 3) 10 in series, 4) 12 in series.

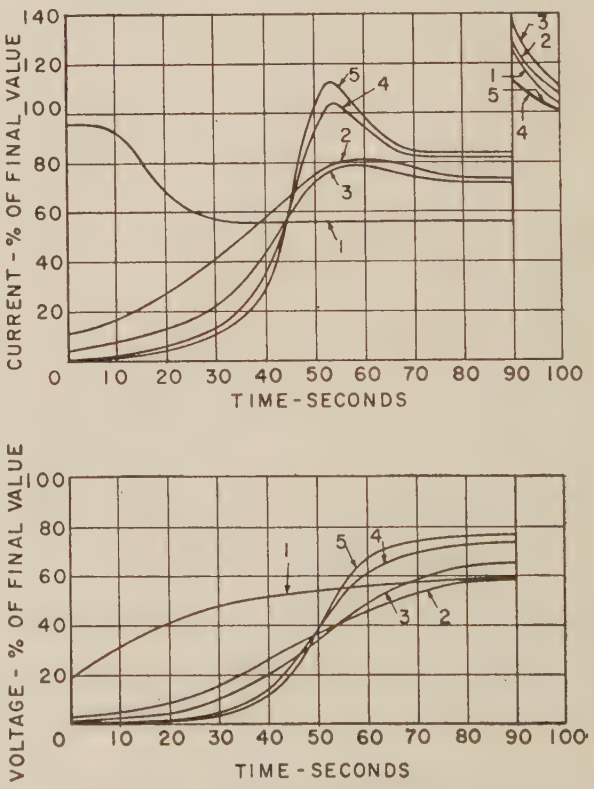

Fig. 4—Filament voltage application. Effect of filament load, 1) 5 per cent load, 2) 30 per cent load, 3) 50 per cent load, 4) 75 per cent load, 5) Full load.

agnitude of the current peaks. With increasing load, e ratio of load resistance to thermistor resistance de-eases, resulting in a lower initial filament voltage. owever, the increased current causes the thermistor to at more rapidly and lower its resistance. These effects nd to cancel each other and allow application of one t of thermistors to a wide range of loads.

Table I gives the most favorable number and type of andard commercially available thermistors, as deter-ined experimentally, for application to various loads to 1100 watts. Grade 1 material is used for lower ads because it has a higher resistivity and a larger mperature coefficient of resistivity than grade 2. This necessary to accommodate the high resistance of the inimum load application. Grade 2 is used for the higher ads because of the more favorable ratio of thermal sponse to resistance.

TABLE I

NUMBER OF THERMISTORS REQUIRED FOR VARIOUS FILAMENT LOADS

ansformer Primary Current Ampere)	Grade of Material*	Washer Thickness†	Thermistor Rating (Ampere)	No. in Series
0–1.5	1	0.145	2.2	4
1.0–4.9	2	0.106	4.8	12
3.0–9.5	3	0.034	8.4	25

* See Appendix for definition of grade of material.
† All thermistors, washer type, 0.75 inch od and 0.28 inch id.

The lack of correlation between the thermistor rat-gs and the transformer primary currents in Table I is result of the effort to obtain the most favorable num-r of thermistors for a wide range of loads. For a par-ular fixed load, the most favorable number of ther-stors might be less than that shown in the table.

Possible Developments

It would be very convenient to reduce the number of ermistors required from that presented in Table I. It s thought that by attaching dissipators to the ther-stor elements, the thermal capacity could be in-eased and the heat extracted faster, thus preventing apid increase in thermistor temperature and reducing e first current peak. However, experiments failed to ow any appreciable improvement. It was deduced at there was insufficient heat conduction in the ther-stor itself. Because of the nonhomogeneities in the ystal structure, a local hot spot develops, decreasing e resistance of this area and increasing the current w, which generates more heat. This progression con-ues until a thermal equilibrium is reached. By electri-lly connecting several thermistors in series, the effect a hot spot in a single or a few thermistors is reduced, sulting in a lowering of the magnitude of the current ak. If the crystal structure of thermistors could be ade more homogeneous, it is very likely that fewer ermistors could be used and dissipators could be ofitably added to increase the current rating.

The elimination of the contactor which shorts out the thermistors would also offer a great advantage in cost and simplicity. The curves of Fig. 3 indicate that the voltage across the thermistor is 25 per cent of the final filament voltage. It would be uneconomical to leave the thermistors in the circuit, consuming 25 per cent of the power. However, assuming a change in thermistor resistance of 100 to 1 and filament resistance of 1 to 5, and designing the circuit so that the initial filament voltage is 10 per cent of the final value, the final filament voltage would be greater than 98 per cent of rated. The thermistors could then be left in the circuit. The drawback is that a circuit so designed with commercially available thermistors makes the magnitude of the first current peak prohibitively large and the increase of filament voltage too rapid. This problem may be overcome by designing a thermistor with large thermal capacity and lower resistance; for example, by increasing the diameter while maintaining the same thickness.

Conclusion

Thermistors can be aptly used for the gradual application of filament voltage in vacuum tubes. Commercially available units can accommodate loads up to 1100 watts. At present, their thermal and electrical properties require that several be connected in series to give the desired voltage response. Based on comparative records between two large-scale digital computers at Massachusetts Institute of Technology (Whirlwind I and the Memory Test Computer), the failure rate of tubes in the computer with no provision for the gradual application of heater voltage was twice that of the computer which uses a motor generator set for the purpose. The number of filament failures, as a percentage of total tube failures was small (only 3.6 per cent) probably due to the fact that ruggedized tubes were used. Although this failure rate would be relatively insignificant in general applications, it becomes important in large computer systems which work around the clock. In such cases, a premium is placed on reliability and any unscheduled computer down-time is a serious problem. A thermistor filament control system will cost approximately 90 dollars per kilowatt to install as against 50 dollars per kilowatt for a system employing resistors, but will be 50 per cent more effective. If, however, the full potentialities of thermistors could be developed so that they could remain in the circuit and thus eliminate contactors, the installed cost of a thermistor system should drop to 10 to 15 dollars per kilowatt. The installation, then, would be economical purely on a cost basis with added reliability as a bonus.

Appendix

Description

Thermistors are thermally-sensitive resistors composed of the powdered oxides of manganese, nickel, and sometimes cobalt, which are pressed into the desired shape and sintered to yield a material whose electrical

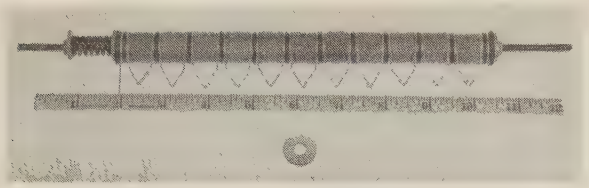

Fig. 5—Thermistor and thermistor assembly.

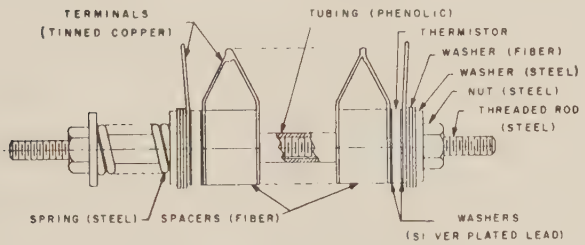

Fig. 6—Mounting for a set of series connected thermistors.

resistance decreases as its temperature rises. The thermal and electrical characteristics can be varied by changing the proportions of the oxides and the sintering temperature. There are two standard mixtures, designated as grade 1 and grade 2 material. Grade 2 material has higher resistivity and a larger negative coefficient of resistance than grade 1 material. While thermistors are made in various sizes and shapes, the washer type is suitable for filament voltage application because of its low ratio of electrical resistance to thermal capacity and its high current rating.

Mechanically, thermistors will withstand very great compressive forces but relatively small tensile forces. Further, thermistors have an appreciable negative temperature coefficient of expansion. Therefore, care must be taken when mounting thermistors that tensile forces are minimized and that allowance is made for the contraction and expansion.

Mounting

The recommended mounting for a set of washer type thermistors is shown in the photograph of Fig. 5 and the drawing of Fig. 6. The lead washers are used to equalize the pressure over the entire flat surface, thus minimizing any tendency to develop tensile forces. Silver plating the surfaces of the lead washer insures good electrical contact with the thermistor. Silver is used instead of tin because the melting point of the lead-tin eutectic is 180°C, and the temperature may reach 200°C when rated current is flowing through the assembly.

The wiring terminal is made the same diameter as the thermistor to equalize the pressure over the surface of the thermistor and to obtain uniform current density throughout the thermistor. The fiber washer and spacers electrically and thermally isolate the thermistors. The spring allows for thermal expansion and contraction while providing sufficient contact pressure. Excessive pressure will cause plastic flow of the lead washer and too little pressure will provide insufficient electrical contact. A satisfactory value for contact pressure has been found to be about 50 pounds per square inch of thermistor surface.

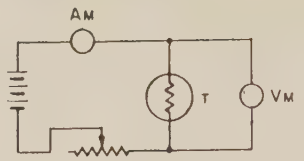

Fig. 7—Circuit for obtaining thermistor current rating.

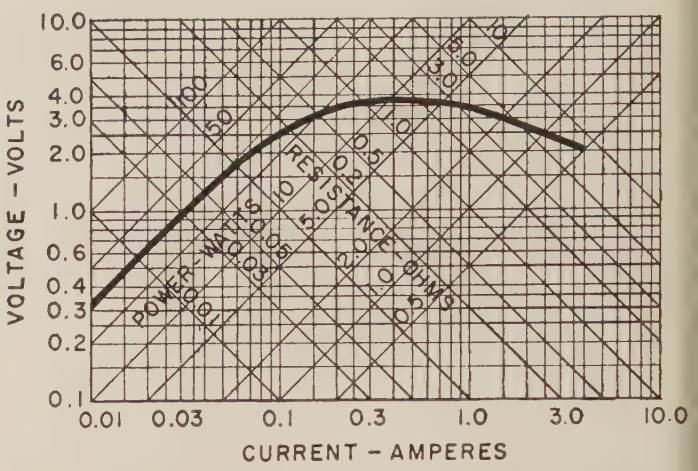

Fig. 8—Typical static volt-ampere characteristic for thermistor.

Rating

The current rating of a thermistor depends upon the type of mounting. The rating may be obtained by placing the thermistor in an oven at 200°C and measuring its resistance. The thermistor is then removed and allowed to cool to the ambient temperature at which it is to be used. It is then mounted as it will be in the final application. Current is then passed through it and slowly increased to such a value that its resistance is reduced to the same value as that obtained by the oven measurement. This value is its current rating for this mounting. A circuit for obtaining the current rating is shown in Fig. 7. The same circuit may also be used to obtain the static volt-ampere characteristic, for which a typical curve is shown in Fig. 8.

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Review of Computer Progress in 1957*

R. P. CASTANIAS† AND J. E. SHERMAN†

I. Digital Computer Progress in 1957

As each year passes it is becoming a little more difficult to accomplish the task of reviewing computer progress for the year. The ever-expanding computer industry has the definite earmarks of becoming one of the largest in existence. In the beginning, when there were only a few computers and as many computing centers, it was easy to note progress. One could merely correspond with these various centers requesting a monthly or yearly progress report and by a brief editing and compiling job, prepare an adequate review. Today, however, we have so many different computers and computing centers that the use of this approach proves rather impractical. A general over-all review can best be accomplished by a quick review of the titles of some of the papers that have been presented at major conferences held during the past year.

As pointed out in the "Review of Electronic Computer Progress During 1956,"[1] "Probably the most noticeable development in the digital computer field over the last year or two has been the extension of the art in the direction of larger, more complex, and more ambitious computer systems." This trend has continued with Sperry-Rand and the LARC; IBM and the STRETCH; and RCA and the BIZMAC, each releasing to the public further information on these gigantic systems. The BIZMAC is the only one actually in the complete hardware stage.

Univac-LARC, the Livermore Advanced Research Computer, is being built for the University of California's Radiation Laboratories at Livermore, Calif. LARC is Remington Rand Univac's newest all solid-state large scale computer, over 100 times faster than today's scientific computers and internally 1000 times faster than today's business data-processing systems. UCRL is actively engaged in preliminary aspects of coding both the input-output processor and main computing unit. Full scale programming and coding is under way and will occupy a major laboratory effort so that there will be little delay in getting the LARC up to full operation.

STRETCH is being built by IBM for installation at Los Alamos Scientific Laboratory. General performance specifications for STRETCH outlined in the contract would make it between 100 and 200 times faster than any comparable general-purpose calculator available today, and also would permit it to solve problems of much greater scope and complexity. As one indication of its capacity, the calculator is planned to operate so that multiplications of 12 to 15 digit numbers will take place at more than 500,000 a second, and additions at about two million a second.

The BIZMAC system was initially designed to meet the requirements of an integrated clerical operation. The over-all design philosophy expressed by the system was to fit to this large-scale data processing a most economical equipment complement. This was accomplished by functionally analyzing studies of operations in public utilities, life insurance companies, government agencies, merchandising firms, and manufacturing firms for the purpose of adapting the equipment of these functions.

Several smaller yet significant systems receiving public notice were the DATAmatic 1000, NCR 304, IBM 705 III and the ALWAC 800.

The DATAmatic 1000 is a high-capacity electronic data-processing system designed specifically for application to the increasingly complex problems and procedures of present-day business. One of the outstanding features of the D-1000 is its ability to feed information from magnetic tape into the central processor at a sustained rate of 60,000 decimal-digits per second, and to deliver data after processing back to magnetic tape at this same rate.

The NCR 304, part of a program to produce a new type of electronic data-processing system for general business use, was announced by the National Cash Register Company. The new system will provide automatic accounting, auditing, reporting, and other business record-keeping functions in one continuous high-speed operation.

The IBM 705 III, designed especially for the large-volume, low-activity application requiring high internal and tape-passing speeds, is one of the most powerful data-processing systems yet developed. While retaining the basic features of earlier 705 systems, the 705 III offers improvements that result in tremendous increases in speed and versatility. The IBM 705 III's magnetic core storage of 40,000 positions is standard in the central processing unit.

In conjunction with the IBM 705 III, the IBM 729 III, a magnetic tape unit used in the new system, reads and writes 60,000 characters a second.

The IBM 767 data synchronizer, also used in the new system, has a two-way channel enabling the system to read and compute, or write and compute, at the same time.

The ALWAC 800 is a high-speed, high-capacity electronic data-processing system combining magnetic core storage, magnetic element logic, and modular construction. It provides core storage, drum storage, magnetic tapes, high-speed paper tape, flexible use of punch card and tabulating machines, keyboard, typewriter, and a high-speed printer. All input and output devices of ALWAC 800 have magnetic core buffers linking them to the processor. This makes possible simultaneous and synchronous operation of input devices and processor.

Another noticeable trend is the continued development of the current large-scale computer: IBM is extending the 704 to the 709 and Sperry-Rand has announced its extension of the 1103A to the 1105. The announcement of two newcomers to the field, Philco's TRANSAC S-2000 and Electro Data's 220, places two more computers in this category. Besides larger memories, faster input-output systems, and the usual general beefing up of the over-all system, each of these systems features a buffering system that either allows simultaneous or concurrent processing of input-output while performing the normal computing functions.

The IBM 709 Electronic Data Processing System has features listed below which give it a versatility which will enable it to be applied to both scientific and business problems:

1) 729 magnetic tape unit
2) Simultaneous reading, writing, and computing
3) Large capacity magnetic core storage, 32,768 words
4) Automatic indexing
5) High-speed arithmetic
6) Automatic floating-point arithmetic.

Remington Rand has continued to extend its Univac Scientific Computing System by the addition of two tape control units which operate in concurrent read, write, or read/write modes. This new development has now been tabbed the Univac 1105 Computing System. The insertion of a single buffer storage unit of 120 words enables the computer to transfer a word in about 18 μsec, and a block of 120 words in less than 2.5 msec. This 2.5-msec transfer occurs every 75 msec for continuously running tape, thus permitting an uninterrupted calculate time in which complex calculations can be performed.

The S-2000 Electronic Data Processing Computer is a parallel machine with 48-digit word length using two's complement binary arithmetic for internal calculations. It uses a single-address instruction with 16 digits for the address and 8 digits for the command, and two independent instructions to a word. The magnetic core memory has a destructive-read cycle of 5 μsec and writes a cycle of 7 μsec. (The read and write cycles can be used either separately or together in sequence.) The S-2000 has an initial memory capacity of 4096 words. Arithmetic speeds (exclusive of memory access time) are as follows: addition or subtraction, average 1.5, minimum 0.5, maximum 6.3 μsec; multiplication, average 60.0, minimum 45.0, maximum 300.0 μsec; and division, average 80.0, minimum 50.0, maximum 300.0 μsec.

* Manuscript received by the PGEC, December 31, 1957; revised manuscript received, January 22, 1958.

† Missile Systems Div., Lockheed Aircraft Corp., Palo Alto, Calif.

[1] IRE Trans. on Electronic Computers, vol EC-6, pp. 55–60; March, 1957.

Philco has also announced the following specifications and features for its TRANSAC S-1000. The S-1000 Scientific Computer is a parallel machine with 36-digit word length using one's complement binary arithmetic for internal calculations. It uses a two-address instruction with two 12-digit addresses, two 3-digit address modifiers, and a 6-digit command with one instruction per word. The magnetic core memory has 12-μsec cycle time and memory capacity of 4096 words; arithmetic speeds (exclusive of memory) are as follows: addition and subtraction, 5.5 μsec; multiplication, average 0.130 μsec, maximum 0.200 μsec; division, 200 μsec.

DATAtron 220 marks a decisive breakthrough in the vital area of computer economics. It offers for the first time the computational and data processing capabilities of giant machines.

Organized as a scientific computer, DATAtron 220 with punched paper tape and automatic floating point, provides a formidable system for high-speed problem solving or data reduction. Organized as a business data processor, DATAtron 220 utilizes an extensive variety of punched-card and magnetic tape machines to handle efficiently the masses of data required in accounting, inventory control, billing, payroll, and other record-keeping functions. Linking a powerful digital computer to powerful input-output facilities, DATAtron 220 extends the proven systems concept pioneered by Electro Data.

In the realm of the medium-sized computer, we notice IBM's continued improvement of the 650 by addition of the IBM 355 random access memory in which any group of data may be reached quickly and directly, without search. Up to four 355 memory units may be connected to the 650 system. Of course, this memory unit is also the basis for the 305 RAMAC (Random Access Memory Accounting Machine) which is built around the IBM disk memory. The 5,000,000 digit memory used in 305 RAMAC was developed at the company's laboratory in San Jose, Calif.

Another medium-sized computer available is the ALWAC III E, which is a low-cost medium-sized data processing system with the following features: magnetic tape, punch cards, and high-speed paper tape input and output. Simultaneous searching on all magnetic tape units is possible. Searching is independent of computation. A magnetic core buffer is used for tape units.

The Univac File Computer System is an electronic data processing system which features the simultaneous operation of a large central computer, a large capacity, random access, magnetic drum memory, and an integrated system of input-output units. The Univac airlines reservations system is based on the Univac File Computer.

FLAC II computer being built for Patrick Air Force Base by Technitrol Engineering Company is now nearing completion. The machine construction is complete and is being checked out. The main computer was scheduled for delivery to Patrick, July 15, 1957 where it was mated to a magnetic core memory manufactured by Telemeter Magnetics, Inc.

Philco was one of the organizations that pioneered the transistorized, large-scale data-processing field with the announcement of the TRANSAC S-1000 two years ago. Here was a concept that became a reality; a reality that revolutionized the computer industry. The utilization of transistors in computers makes possible miniaturization, low-power consumption with practically no heat dissipation, and yet performs the processing of business data in microseconds.

Another contribution in this field is made by the construction of the TX-2 computer at the Lincoln Laboratory of M.I.T. which is part of the Lincoln program for the study and development of large-scale digital computer systems. The TX-2 incorporates several new developments in high-speed transistor circuits, large capacity magnetic-core memories, and flexibility in machine organization, and is designed to work efficiently with many input-output devices of different types. In the course of developing the TX-2, Lincoln has constructed a small self-checking multiplier system which is on life test, and a complete, though skeletal, general-purpose computer known as the TX-0 which is now in operation.

A revolutionary new method of computer design has been employed in the development of the X-308 computer, Remington Rand Univac's newest digital computer. By using the Univac Scientific to do the bulk of the detailed design work, Univac engineers have literally caused a "computer to design a computer." This technique, called mechanized design, not only speeded up the development program by several months, but permitted an operational check on the X-308 computer's logic, entirely through simulation.

The first production model of IBM's all-transistor computer has been delivered. The new completely transistorized computer is IBM's 608, an intermediate range machine which operates without the use of a single vacuum tube. Manufactured at the company's plant in Poughkeepsie, N. Y., the machine is the first 608 to come off the IBM assembly line for delivery to a customer.

The new 608 replaces an earlier vacuum tube machine, the IBM 607 calculator. The new unit has more than twice the computing speed and over twice the storage capacity of its predecessor.

RECOMP, a transportable, midget computer, has been designed and developed by Autonetics, a division of North American Aviation, Inc. The first model of this general-purpose, all-transistor digital computer, designated CP-266, has been produced and delivered to the U. S. Air Force Rome Air Development Center.

Along with the ever-increasing list of new large, medium, and small digital computers, we could list the old reliable computers that are being updated to keep abreast of the current trends forward by the newer machines. This task, however, is rather lengthy and it is best to assume that most computing centers that are keeping their computers active, are also updating them continuously.

The Naval Proving Ground, Dahlgren, Va. has announced the retirement of the Aiken Relay Calculator (MARK II), in operation since 1948.

The following is a summary of papers presented at the major computer conferences during 1957.

Systems

"Univac-Larc, the Next Step in Computer Design," J. P. Eckert, Remington Rand.

"Design Objectives for the IBM Stretch Computer," S. W. Dunwell, IBM Corp.

"The RCA Bizmac II—Characteristics and Applications," J. A. Brustman, H. M. Elliott, and A. S. Kranzley, RCA.

"A New Large-Scale Data-Handling System, DATAmatic 1000," J. E. Smity, DATAmatic Corp.

"Functional Description of the NCR 304," M. Shiowitz and A. A. Cherin, Electronics Div., National Cash Register Co.; M. J. Mendelson, Norden-Ketay.

"Advanced Techniques in Univac Scientific Computer Systems," A. A. Cohen, Remington Rand Univac.

"The Philco S-2000 Transistorized Large-Scale Data Processing Systems," S. Y. Wong, Philco Corp.

"The Transac S-1000 Computer," J. B. O'Toole, Hughes Aircraft Co.; J. L. Maddox and S. Y. Wong, Philco Corp.

"The Lincoln TX-2 Computer Development," W. A. Clark, Lincoln Lab., M.I.T.

"TX-0, A Transistor Computer with a 256 by 256 Memory," J. L. Mitchell and K. H. Olsen, M.I.T.

"The RAMAC Data-Processing Machine: System Organization of the IBM 305," M. L. Lesser and J. W. Haanstra, IBM Corp.

"Logical Organization of the Digimatic Computer," J. Rosenberg, Electronic Control Systems, Inc.

"Systems Design of a Dual Computer System," L. S. Michels, Bendix Computer Div., Bendix Aviation Corp.

"Design of a Small, Low Cost, Business Computer," A. B. Churchill, Monroe Calculating Machine Co.

"New Computer Developments Around the World," E. S. Calhoun, Stanford Research Institute.

"The Logistics Research Model 800 Computer," N. Block, Logistics Research, Inc.

"The Tradic Leprechaun Computer," J. A. Githens, Bell Telephone Laboratories, Inc.

"Computers with European Accents," A. L. Samuel, IBM Corp.

"Recent IBM Developments in High Speed Computation and Design Objectives for the Super Speed Stretch Computer," J. L. Greenstadt and S. W. Dunwell, IBM Corp.

"A Magnetic Matrix Computing System," G. A. Oliver, Burroughs Corp. Research Center.

"Modern Trends in Digital Computer System Design," W. F. Bauer, Ramo-Wooldridge Corp.

Data Processing

"Sage—A Data Processing System for Air Defense," R. R. Everett, C. Z. Zraket, and H. D. Bennington, Lincoln Lab., M.I.T.

"The Utilization of Domain-Wall Viscosity in Data-Handling Devices," V. L. Newhouse, RCA.

eal-Time Data Processing for CAA Air Traffic Control Operations," G. E. Fenimore, CAA Technical Development Evaluation Center.
rborne Data Acquisition—Ground Based Data Processing System," W. H. Foster, Electronic Engineering Co. of Calif.
esign Techniques for Multiple Interconnected On-Line Data Processors," F. J. Gaffney and S. Levine, Teleregister Corp.
utomatic Input for Business Data-Processing Systems," K. R. Eldredge, F. J. Kamphoefner, and P. H. Wendt, Stanford Research Institute.
ata Processors for Information Retrieval Purposes," S. N. Alexander, National Bureau of Standards, Washington.
volution of a Data Processing System," W. Waddell, Daystrom Systems.
he Variable Word and Record Length and the Combined Record Approach on Electronic Data-Processing Systems," N. J. Dean, Ramo-Wooldridge Corp.

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Large-Capacity Drum-File Memory System," H. F. Welsh and V. J. Porter, Remington Rand Univac.
Medium-Speed Magnetic Core Memory," G. E. Valenty, Remington Rand Univac.
uasi-Random Access Memory Systems," G. L. Hollander, Clevite Research Center.
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Cryotron Catalog Memory System," A. E. Slade and H. O. McMahon, A. D. Little, Inc.
he IBM 650 RAMAC System Disk Storage Operation," D. Royse, IBM Corp.
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Magnetic Tape File Processing with the NCR 304, a New Business Computer," J. S. Sumner, National Cash Register, Inc.
n Approach to Design of Recording Systems for Computer Use," R. C. Hix and E. G. Wildanger, Ampex Corp.
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he Lincoln TX-2 Input-Output System," J. W. Forgie, Lincoln Lab., M.I.T.
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"A New Input-Output Selection System for the Florida Automatic Computer (FLAC)," C. F. Sumner, RCA Missile Test Project.
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"A Method of Coupling a Small Computer to Input-Output Devices without Extensive Buffers," J. H. Randall, National Cash Register Co.

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"Transistor Circuitry in the Lincoln TX-2," K. H. Olsen, Lincoln Lab., M.I.T.
"A Technique for Using Memory Cores as Logical Elements," L. J. Andrews, Electronics Div., National Cash Register Co.
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"A Magnetically Controlled Gating Element," D. A. Buck, M.I.T.
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II. Analog Computer Progress in 1957

The big news of 1957 regarding analog computers is the advent of the digital control unit. All of the major computer manufacturers now offer a method of setting up, programming, checking, and reading out information by means of electric typewriters and punched paper tape. The attached description of the DO/IT System, which is manufactured by the Berkeley Division of Beckman Instruments in conjunction with their EASE Computer, is typical of the type of digital control now available.

DO/IT System

The following major functions may be accomplished by this system, any of which may be controlled from a punched-tape program of instructions, or from an input keyboard:

1) The setting of coefficient potentiometers, with printout of value set.

2) The reading of coefficient potentiometers, with printout of coefficient value read, and the punching of a program tape of set instructions containing the values read.

3) The scanning of one or more points in the computer, chosen from a set of points previously connected to the selector switch, with printout of the voltage and sign at the addressed point.

4) Operation control of computer, to place it into Initial Condition, Compute, Static Check, or Integrator Check states.

A program formed of the proper combinations of instructions, which initiate and control the various functions, will permit the convenient accomplishment of the following modes of operation:

1) The setup and reading of potentiometer coefficients, and in particular, the transferral of set values to the external tape memory, which permits the clearing of the computer for other work, with the ability to later conveniently reinsert the original problem values.

2) The systematic change of coefficients and recomputation to automatically program survey-type investigations.

3) The printout of result function at any desired computation interval (as set on the digital clock of the computer) forming a tabular output to the full accuracy of the computer.

4) Use of formalized methods of checking after problem setup.

5) Use of formalized maintenance procedures, since the scanned points may include supply voltages, test points, etc.

6) Semiattended operation of the computer during long problems.

The list of instructions used to control the functions of the standard DO/IT is as follows.

Code	Instruction	Response	Description
(s)	code-address-value s105 8792	105 8791	Set one coefficient potentiometer; read value to which set, and compare with value ordered by instruction. If they differ by more than 20 mv, print response value in red.
(r)	code-address r105	s105 8791	Read one coefficient potentiometer; read and print value. Also punch a Set instruction, if desired. (Flexowriter in tape punch condition.)
(r)	code-start address- end address r105 107	s105 8791 s106 2424 s107 6500	Read the number of coefficient potentiometers included between the first and second addressed; print (and punch) responses.
(a)	a105	a105 24.21	Scan one amplifier output. The value scanned may be positive or negative in sign, and if over 100 v, format control will maintain column lineup on printout.
(a)	a105 107	a105 24.21[2] a107 104.6	Scan the number of amplifiers included between the addresses. In this multiple form of the instruction, a test is made to determine whether the addressed point is within 20 mv of zero volts, and if so, this point is skipped in the response, with resultant saving in printout time.
(m)	Scan one or more multiplier outputs, same form as (a) instruction. Servo outputs will pass to as many as five scan address points for each unit.		
(f)	Scan function generator outputs, same form as (a) instruction.		
(t)	Scan trunks, or miscellaneous test voltage points, in same form as (a) instruction.		
(x)	This is a free class of scan points, which may be connected as required in the individual installation.		
(u)		a000 24.21 a001 05.94 — a050 12.12 m000 01.59 m001 99.02 — etc.	Scan all valid addresses of all classes. These points are scanned in a, m, f, t, x order, starting at address 000 in each class and proceeding to a maximum limit address which is wired into the scan switch for each installation. Skipping of points near to zero volts will occur, as in (a) instruction.
(i)		none, except carriage return.	Places computer into initial condition state. A two-second delay incorporated to permit settling.
(c)	c	same as (i)	Places computer into Compute state. A five-second limit on the Precompute state (if energized) is checked by a timer; then the instruction will be completed by the transfer of computer to Hold state, as the end of the period set into the digital clock, or by operational relay, or operator.
(k)	k	same as (i)	Places computer into Static Check state. A thirty-second delay is incorporated to permit settling.
(j)	j	same as (i)	Places computer into Integrator Check state. A thirty-second limit on this instruction is completed upon transfer of computer to Hold state.
(d)	d	same as (i)	Disconnects DO/IT system from computer, for insertion of memoranda onto printed copy or onto a program tape.
(P1)	none	same as (i)	Reconnect DO/IT system, after memorandum, for insertion of further instructions.
STOP)	none	none	A special key on Flexowriter. When this character is inserted in program tape, DO/IT unit will operate Stop Alarm to call operator for manual insertions into program, or other required attention.

[2] Assume a106 value was −00.02.

The major analog computer manufacturers and their digital control unit code names are:

Company Name

1) Beckman/Berkeley
2) Electronic Associates, Inc.
3) Goodyear Aircraft Corp.
4) Mid-Century Instrumatic Corp.
5) Reeves Instrument Corp.

Computer Designation

1) EASE 1132
2) PACE 231-R
3) GEDA A-14
4) MC 5800
5) REAC 400

Digital Control Designation

1) DO/IT
(Digital Output-Input Translater)
2) ADIOS
(Automatic Digital Input-Output System)
3) Problem Analyzer
4) DIGI-SCAN
5) Auto Control System

While all of the companies offer digital control units, there are some differences in some of the accessory features. For example, the GEDA problem analyzer does more than merely read out amplifiers. It actually traces the signal from each amplifier through to all the points where that signal goes and prints out not only the information as to where the signal goes, but also the gain involved.

The Reeves Instrument Company has a device that indicates which amplifiers have signals which always remain below an arbitrarily set level.

All of the major computer manufacturers now offer operational consoles containing approximately 100 amplifiers plus assorted nonlinear equipment.

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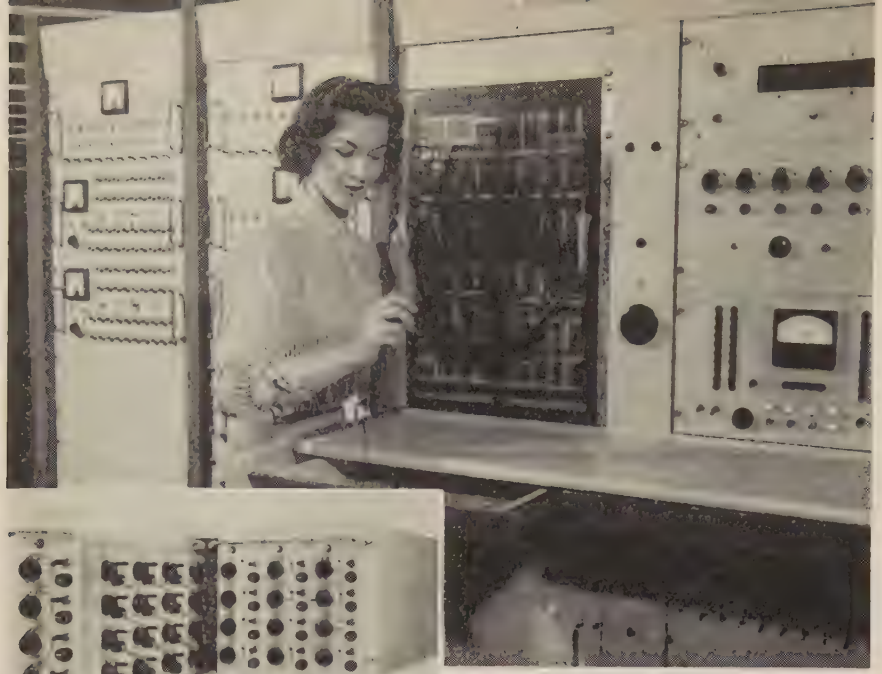


EASE 1132 computer with DO/IT system

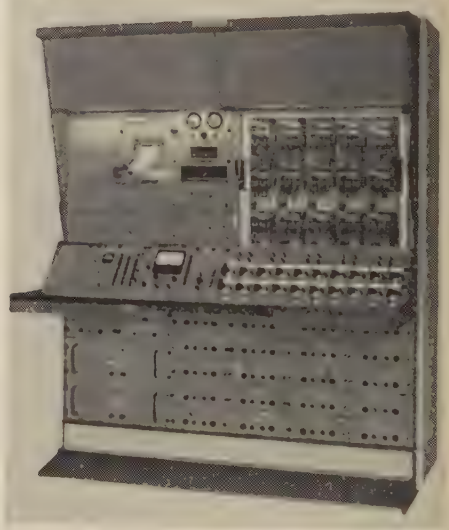
REAC autocontrol system.

New method of packaging manually set potentiometers developed by Beckman/Berkeley for EASE computer.

Automatic control console for Electronic Associates' PACE computer.

REAC 400 computer with autocontrol system

Midcentury Instrumate MC 5800 computer



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Addenda

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[94] Kirchmayer, L. K. "Differential Analyzer Aids Design of Computer Control System for Electric Utilities."
[95] Chestnut, H. and Leiby, D. W. "Analog Computer Study of Sampled Data Systems."
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Contributors

R. D. Berlin (A'55) was born in Newark, N. J. on November 1, 1924. He received the B.S. degree in electrical engineering from Newark College of Engineering in 1948. In 1949 he received the M.S. degree in mathematics from Syracuse University where he has also completed his course requirements for the Ph.D. degree in mathematics.

From 1944 to 1946 he was engaged in radio and radar maintenance and installation in the U. S. Navy. From 1949 to 1951 he taught in the Department of Mathematics at Syracuse University. Since 1951 he has been employed at the Electronics Laboratory of the General Electric Company, in Syracuse, N. Y. His work there is concerned with systems, digital computer design, and switching theory.

Mr. Berlin is a member of the Association for Computing Machinery and the American Mathematical Society.

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Richard P. Castanias was born in Spokane, Wash. on May 25, 1925. He received the B.S. degree in electrical engineering and mathematics from the University of Toledo, Toledo, Ohio in January and June, 1949, respectively. He received the M.S. degree in mathematics from Purdue University, Lafayette, Ind. in 1951. He has taught physics at the University of Toledo and mathematics at Purdue University while obtaining his degrees.

He entered the Marines in 1942 where he attended radar school and later taught radar fundamentals, prior to an extended overseas tour. Following his service in 1946, he worked for the Naval Research Laboratories, Washington, D. C.

From 1951 to 1953 Mr. Castanias headed the engineering IBM group at Chance Vought Aircraft, Dallas, Tex. From 1953 to 1956 he headed the mathematics department for the Vitro Corporation of America at Eglin Air Force Base, Fla. He has been with Lockheed Missile Systems Division, Lockheed Aircraft Corporation, since 1956 and is currently manager of the Math and Computer Services Department.

Mr. Castanias is a member of the Association for Computing Machinery, Society for Industrial and Applied Mathematics, and the American Ordnance Association.

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Paul C. Dow, Jr., for biography, please see page 288 of the December, 1957 issue of these TRANSACTIONS.

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James W. Easley was born November 17, 1922 in Los Angeles, Calif. He received the A.B. degree in 1950 and the Ph.D. degree in 1955 in physics from the University of California.

Before joining Bell Telephone Laboratories in 1954, Dr. Easley was employed at the Radiation Laboratory of the University of California at Berkeley. Since joining Bell Telephone Laboratories, he has been engaged in transistor characterization and the application of solid-state devices to digital computer circuitry.

Dr. Easley is a member of the American Physical Society and Sigma Xi.

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George Epstein (S'57) was born on July 4, 1934 in Bayonne, N. J. He received the B.S. degree from the California Institute of Technology in 1955 and the M.S. degree in mathematics from the University of Illinois in 1957.

Mr. Epstein was a teaching assistant in mathematics at the University of Illinois from 1955 to 1957. During the summer of that period he was employed by Hycon Manufacturing, where he worked in the development of pulse circuitry.

At present he is a member of the technical staff in the Computing and Controls Department of the Airborne Systems Laboratories, Hughes Aircraft Company, and is a Ph.D. candidate at the University of California at Los Angeles.

He is a member of the Association for Computing Machinery, Mathematical Association of America, and Pi Mu Epsilon.

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J. J. Gano (SM'57) was born in Boston, Mass., on January 13, 1913. He received the S.B. degree in mechanical engineering from Harvard University, Cambridge, Mass. in 1935 and the S.M. degree in electrical engineering from the Massachusetts Institute of Technology, Cambridge in 1952.

He was employed for three years in the research laboratories and the air conditioning department of Westinghouse Electric Corporation. From 1938 to 1941 he was a development engineer on steam turbines and industrial burners with Coppus Engineering Corporation, Worcester, Mass. Following this he worked on automatic controls for machine tools at Controls Laboratories, Worcester, Mass. In 1948 he joined the staff of the Digital Computer Laboratory of M.I.T. and later Lincoln Laboratory of M.I.T. where he was a section leader on power and controls in the digital computer division. In early 1952 he left to organize J. J. Gano and Associates, a consulting service on power systems for electronic equipment.

Mr. Gano is a member of AIEE, ASME, Tau Beta Pi, and Sigma Xi.

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J. R. Harris (A'43–M'49) was born in Lockhart, Tex. in 1920. He received the B.S. degree in physics from the University of Richmond in 1941. After a year in the Engineering Department of the Chesapeake and Potomac Telephone Company of Virginia, he joined Bell Telephone Laboratories to develop airborne radiotelephone and navigation equipment. He received the Master of Electrical Engineering degree from Polytechnic Institute of Brooklyn in 1948. In 1950 he joined a group concerned with the development of transistors and packaged switching circuits based on transistors. He was one of the members of the TRADIC computer project, sponsored by the Air Force, when it was formed in 1951. Since 1956 he has been associated with Bell System data processing development.

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Harry D. Huskey (A'49–M'55) was born in Whittier, N. C. on January 16, 1916. He received the B.S. degree from the University of Idaho in 1937, the M.A. degree in 1940, and the Ph.D. degree in 1943, both from Ohio State University.

During the years 1943–1946, he was an instructor at the University of Pennsylvania at Philadelphia, where he worked on the ENIAC. In 1947, he worked at the National Physical Laboratory, Teddington, England, where he did research in coding and logical design for digital computing machines, supervised the design, and began the actual construction of a pilot model of the ACE, a stored-program computer using mercury delay lines for the memory unit. In 1948, he returned to the National Bureau of Standards in Washington, D. C., where he became chief of the Machine Development Laboratory of the National Applied Mathematics Laboratories. In December, 1948, he was transferred to the Institute for Numerical Analysis, a field station of the National Bureau of Standards, located at Los Angeles. There he was responsible for the design and construction of the National Bureau of Standards Western Automatic Computer (SWAC). In 1950, Dr. Huskey became assistant director in charge of Mathematical Services at the Institute and in September, 1952, he obtained a year's leave of absence to become the Technical Director of the Computation Laboratory of Wayne University, Detroit.

Dr. Huskey helped to organize and was the first Chairman of the Professional Group on Electronic Computers in the Los Angeles area and served as the first Vice-Chairman of the National Professional Group. He has been editor of the review section of these TRANSACTIONS.

In September, 1954, he was appointed associate professor of mathematics and electrical engineering at the University of California, Berkeley, Calif. At the invitation of the Dutch Government, he spent the summer of 1955 at the Mathematische Centrum, Amsterdam.

Dr. Huskey is a member of the Association for Computing Machinery, the American Mathematical Society, the Mathematical Association of America, the Industrial Mathematical Society, and Sigma Xi, and is a Fellow of the American Association for the Advancement of Science.

Jack M. Maughmer (A'53) was born in Spokane, Wash. on January 18, 1926. After serving in the U. S. Air Force from 1944 through 1945, he entered the University of California and received the B.S. degree in electrical engineering in 1949. During his employment with International Business Machines Corporation he received the M.S. degree in electrical engineering in 1954, also from the University of California.

From September, 1954 to January, 1957, he pursued his doctoral studies as a research engineer in the Computer Laboratory at the University of California, receiving the Ph.D. degree in electrical engineering in January, 1957.

At present Dr. Maughmer is a senior research engineer at Convair-Astronautics in San Diego, Calif.

He is a member of Sigma Xi and is a registered electrical engineer in the state of California.

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George E. McDuffie, Jr. (M'53) was born on April 4, 1925 in Washington, D. C. He received the B.E.E. degree in 1949 and the M.E.E. degree in 1952, both from the Catholic University of America in Washington, D. C. He is presently engaged in additional graduate study at the University of Maryland.

Since receiving the Bachelor's degree Mr. McDuffie has been teaching on the faculty of the Catholic University of America and is now assistant professor in the Department of Electrical Engineering. For the past five years he has also been active in the ferroelectric research program at Catholic University, particularly on the application of ferroelectrics in the computer field.

Mr. McDuffie is a member of Sigma Xi and the American Society for Engineering Education.

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Amos Nathan, for biography, please see page 125 of the June, 1957 issue of these TRANSACTIONS.

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Charles F. Pulvari (SM'54) was born in Karlsbad, Austria-Hungary in 1907. He received his diploma in electrical and mechanical engineering at the University of Technical Sciences in Budapest. After graduation, he was associated with the Research Laboratories of the Telephone Manufacturing Company in Budapest for three years. Professor Pulvari then joined Hungary Radio and Communications Company as Chief Engineer. Later, he became Technical Director.

In London he became a consultant on television for Scophoney, Limited. After World War II, he organized his own research laboratory in the switching and communications field and began research in solid-state physics. He came to the United States in 1949, and joined the George Washington University, where he pursued research on electrostatic information devices. Professor Pulvari later became a member of the staff of the Catholic University of America and is, at this time, professor of electrical engineering and head of the Computer Research Laboratory. He has contributed to development of ferroelectric memory devices using single capacitors and holds numerous U. S. patents.

Professor Pulvari is a member of Sigma Xi.

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G. F. Sandy was born on August 5, 1926, in Shinnston, W. Va. He was selected for officer training in the Navy V-12 program in 1944, receiving the B.E.E. degree from the University of Louisville, Ky. and a commission in the U. S. Naval Reserve in 1947. He attended the graduate school of Case Institute of Technology, Cleveland, Ohio until 1948.

He worked at the Packard Electric Division of General Motors Corporation in the Plant Engineering and Product Engineering departments. Since 1952, he has been a staff member of the Lincoln Laboratory of the Massachusetts Institute of Technology, where he has worked on power supply, distribution and control problems of large scale digital computers. He is now concerned with digital circuit development for the SAGE air defense system.

Mr. Sandy is a member of Sigma Tau.

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Hermann Schmid was born in Kempten, Germany on March 19, 1925. In 1950 he graduated from the Staatstechnikum (State Technical College) Konstanz, Germany with the degree of Electrical Engineer. From 1951 until 1956 he was with Computing Devices of Canada Limited where, during the last three years, he worked as Project Engineer on a weather simulator for a tactical trainer.

In 1956, Mr. Schmid joined Link Aviation, Inc. in Binghamton, N. Y. where he has been engaged in the development of analog computing circuitry.

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John E. Sherman (M'58) was born on January 18, 1922 in Brooklyn, N. Y. He attended Hofstra College in Hempstead, N. Y. where he received the A.B. degree in mathematics and physics in 1950. During 1950 and 1951 he did graduate work in physics at the University of Oklahoma. From 1951 to 1952 he was employed by the U. S. Naval Air Missile Test Center at Point Mugu, Calif., where he operated an analog computer. In 1953 and 1954 he was in charge of the analog computer installation at McDonnell Aircraft Corporation in St. Louis, Mo. Since 1953 he has been in charge of all the analog computer installations in the Lockheed Missile Systems Division, Palo Alto, Calif.

During 1956 and 1957 Mr. Sherman was the Chairman of the Western Simulation Council. He is currently a member of the Board of Directors of Simulation Councils, Inc.

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Rajko Tomovich was born in Baja, Hungary, on November 1, 1919. He graduated from the Electrical Engineering Department of the University in Belgrade in 1946.

After graduation he joined the Power Engineering Institute in Belgrade, where he was engaged in designing computers for the study of electrical transmission systems.

He spent the summer of 1950 at the Massachusetts Institute of Technology as the Yugoslav participant of the Foreign Student Summer Project and in 1952, received the Doctor's degree in Belgrade for research work in analog computers. He joined the Boris Kidrich Institute of Nuclear Sciences, Belgrade, Yugoslavia, in 1951 as research associate of the Laboratory of Applied Mathematics where he is presently head of the Institute's Digital Computer Department.

Dr. Tomovich is a member of the provisional governing committee of the International Association for Analog Computation, as well as a member of its editorial board.

PGEC News

ATIONAL SIMULATION ONFERENCE

The 1958 National Simulation Conference, sponsored by the Institute of Radio ngineers Professional Group on Electronic omputers and the Dallas Section of the stitute of Radio Engineers, will be held in allas, Texas, October 23–25, 1958, at the atler-Hilton Hotel.

Technical papers in the general field of mulation are hereby solicited. Papers subitted must not have been previously preinted at a meeting of national scope nor reviously published in a nationally cirulated journal. One hundred word abracts and 500 word summaries, to aid in aper selection should be transmitted in uplicate to the Technical Program Chairan: D. J. Simmons, Route 8, Box 447, Fort Worth, Texas. *The deadline is June 25, 1958.*

In addition to topics such as the analog nd/or digital simulation of mathematical, hysical, logistic, economic, biological, and nemical systems, papers are desired coverg advances in analog computer system nd component design, techniques, and pplications, as well as new methods of dermining and improving the accuracy of nalog solutions.

No "proceedings" volume will be pubshed as such, but authors of papers acpted for the Conference will be expected submit the full text of their papers to the RE TRANSACTIONS ON ELECTRONIC COMUTERS for consideration for publication in hat journal.

EW YORK CHAPTER PGEC LECTS OFFICERS

The New York Chapter PGEC has lected the following officers for 1957–1958:

Chairman, M. J. Relis, Control Instrument Company
Vice-Chairman, P. E. Magdeburger, International Business Machines Corporation
Secretary-Treasurer, R. Stella, W. L. Maxson Corporation.

ENTH SOUTHWESTERN IRE CONERENCE AND ELECTRONICS SHOW

The Tenth Southwestern IRE Conference and Electronics Show will be held in Austin, Texas at the St. Anthony Hotel and Municipal Auditorium on April 10–12, 958. The deadline for papers has passed, ut further information about the meeting nay be obtained from Dr. William H. Hartwig, P. O. Box 7948, University Station, Austin 12, Texas.

1958 WESCON CONVENTION

Authors wishing to present papers at the 1958 WESCON Convention to be held in Los Angeles on August 19–22 should send 100-word abstracts and either the complete text or a detailed summary to the Technical Program Committee Chairman: Dr. Robert C. Hansen, Microwave Laboratory, Hughes Aircraft Co., Culver City, Calif. *The deadline is May 1, 1958.*

There will again be an IRE WESCON CONVENTION RECORD. Authors will be notified of acceptance or rejection by June 1.

THE BRITISH GROUP FOR COMPUTATION AND AUTOMATIC CONTROL OF THE BRITISH CONFERENCE ON AUTOMATION AND COMPUTATION

The British Conference on Automation and Computation has been established as follows:

The British Group for the Engineering Applications of Automation.
The British Group for Computation and Automatic Control.
The British Group for the Sociological and Economic Aspects of Automation Techniques.

The British Group for Computation and Automatic Control has been formally constituted, comprising as its members the following societies:

British Computer Society
Chartered Institute of Secretaries
Chemical Society
Faculty of Actuaries (Scotland)
Institute of Actuaries
Institute of Bankers
Institute of Chartered Accountants in England and Wales
Institute of Chartered Accountants of Scotland
Institute of Cost and Works Accountants
Institute of Fuel
Institute of Municipal Treasurers and Accountants (Incorporated)
Institute of Petroleum
Institute of Physics
Institution of Civil Engineers
Institution of Electrical Engineers
Institution of Mechanical Engineers
Institution of Production Engineers
Iron and Steel Institute
Office Management Association
Royal Aeronautical Society.

Communications about the British Group for Automation and Automatic Control should be addressed to the Honorary Secretary, BCAC, Group B, c/o Institution of Electrical Engineers, Savoy Place, London, W.C. 2.

SUMMARY OF THE ADMINISTRATIVE COMMITTEE MEETING DECEMBER 12, 1957, WASHINGTON, D. C.

A quorum of twelve members or proxies was represented at the meeting in addition to Committee Chairmen and Chapter Chairmen.

A report was presented on the progress of the International Conference on Information Processing Systems. I. L. Auerbach, who is PGEC representative at this conference, was about to leave for Paris to attend an organizing meeting. Since the meeting, he has reported that excellent progress was made in Paris and that the International Conference is now firmly established for the summer of 1959. It is to be held in Paris under the sponsorship of UNESCO.

The PGEC approved the charter of the National Joint Computer Committee, with the exception that it voted to eliminate standardization in the computer field as an activity for the JCC. It was felt that this is a matter for each professional society to carry on, and the IRE has a strong standardization activity already.

The IRE Computer Fellowship was administered by the National Science Foundation last year, but the Foundation indicated it would be unwilling to continue. R. W. Melville is working on a new arrangement, but in the meantime the Fellowship may have to lapse for one year.

Secretary-Treasurer H. W. Nordyke presented a financial statement indicating that the balance in the PGEC treasury continued to increase. The Administrative Committee is continuing to look for worthwhile activities which the PGEC should sponsor with these funds.

Past Chairman Jerre D. Noe is heading the Nominations Committee, together with two members of the Administrative Committee and two of the Chapter Chairmen.

Because the Western Joint Computer Conference has been moved from February to May, 1958, the customary Administrative Committee meeting in February on the West Coast has to be omitted. The next meeting of the Administrative Committee will be held during the IRE Convention in March.

W. Buchholz
Chairman

SECOND INTERNATIONAL CONFERENCE FOR ANALOG COMPUTATIONS

The Second International Conference for Analog Computations is to be held at Strasburg on September 1, 1958.

This Conference, which will last one week, will be devoted to the various systems of analog computations, their numerous ap-

plications, and the connections between analog methods and arithmetic methods of computation in electronics.

The subject will be divided into four sections:

Theoretical, mathematical, or physical problems
Analog computation materials
Diverse and similar applications
Connection between analog computers and arithmetic calculators.

The Organization Committee is looking for papers on present construction techniques and the employment of analog computations. These will be published subsequently in the Acts of Congress.

Further, papers concerned with more limited problems are also requested. The authors are requested to summarize their subject in less than 600 words. All these summaries will be translated into three languages—French, English, and German—and distributed to the members of the Conference on their arrival at Strasburg. Thus each member will be well informed and will be prepared for an exchange of views.

It is intended to hold an exhibition of new equipment adjacent to the conference rooms between August 30th and September 8th.

The Organization Committee would be glad to hear as soon as possible from individuals and companies who plan to participate in the Conference, as well as the nature of their participation: exhibitor of products, author of summary, or auditor. This information should be forwarded to the following address:

M. F. H. Raymond
Secrétaire Délégué Général de l'Association Internationale pour le Calcul Analogique c/o S.E.A.
138, Boulevard de Verdun
Courbevoie (Seine) France.

Call for Papers on Sequential Transducers

A special issue of the IRE Transactions on Circuit Theory tentatively scheduled for March, 1959, will be dedicated to papers on sequential transducers. This relatively new study forms a theoretical basis for the understanding of the capabilities of switching circuits and digital computer control, and coding circuits. Suitable topics for papers submitted for consideration will include:

1) algebra for the terminal description of binary filters,
2) studies of the memory requirements of sequential circuits,
3) interrelationships between finite-state transducers and Turing machines,
4) linear and nonlinear recursive functions and sequence filters,
5) internal circuit redundancy for purposes of terminal error-corrections, and
6) application of old and new synthesis methods to sequential circuits using transistors, magnetic cores, and superconductive elements.

Emphasis will be placed on general theoretical techniques rather than the design of specific equipment.

All decisions by the Editorial Committee as to the suitability of papers submitted for publication in the "Sequential Transducers" issue will be made by November 1, 1958. Papers initially submitted in extended abstract form (about 1000 words) by July 15, 1958 will be given priority of consideration. In any case the deadline for papers, complete with standard abstract and drawings suitable for reproduction, will be December 1, 1958. The preparation of manuscripts should follow the suggestions in "Preparation and Publication of IRE Papers," which appeared on pages 1604–1605 of the November, 1954 issue of the Proceedings.

Please address all correspondence about the "Sequential Transducers" issue of the PGCT Transactions to David A. Huffman, Department of Electrical Engineering, Massachusetts Institute of Technology, Cambridge 39, Mass.

Reviews of Current Literature

In July, I resigned as review editor, effective this issue. Therefore, I would like to thank all those who have participated in the project since its beginning in the September, 1953 issue. I would like particularly to thank my wife for the many hours she has spent helping with the reviews.—*H. D. Huskey*

GENERAL

1-52 58-1

Man as a Link in Complex Machine stems—G. H. Mowbray. (*Sci. Mon.*, vol. pp. 269–276; December, 1956.) The per- mance, particularly the speed of re- nse, of man as a series or parallel link in a ntrol system is discussed. Instrument dials oviding the input to the link and control vices receiving its output should be de- ned to facilitate rapid reading and opera- n, respectively.

Courtesy of Proc. IRE and *Wireless Engineer*

58-2

Guide to Instrumentation Literature—G. Brombacher, Julian F. Smith, and man M. van der Pol. (NBS Circular 567, S. Gov't Printing Office, Washington, C., iv+156 pp.; 1955.) A bibliography ting pertinent works in instrumentation. includes sections on automatic control, alog and digital computers, and many er applications more or less related to mputation. Books and reference works ich appeared no more than about twenty rs prior to the compilation of the bibliog- phy and all periodical articles found were ed. The closing date is not stated, but it s presumably some time during 1954. urces of material are generally described d listed as specifically as is reasonable.

C. B. Tompkins

Courtesy of *Mathematical Tables and Other Aids to Computation*

58-3

Evaluation of New Computer Compo- nts, Equipments, and Systems for Naval e—L. D. Whitelock. (*Proc. Eastern int Comp. Conf.*, December 10–12, 1956, Y., pp. 9–12; 1957.) In this article, L. D. hitelock outlines the criteria used by the ureau of Ships to evaluate computers for val use stressing the broad categories in ich the Navy is interested. These include ore-based commercial computers, shore- sed military computers, and shipboard mputers for use both as R&D and opera- nal units. He points out that the designer any solid-state computers should keep mind 9 basic criteria. These are: What is e function to be performed? Will the uipment adequately meet all of the func- nal requirements? Will the equipment rform in the environment? Can it be de- ered in a time period which will be useful the Navy? Has technical feasibility been oven? Will there be a particularly difficult istics support problem? Will the maintenance problem require special training? Is the design philosophy conservative? Will the cost be comparative with the other possible approaches to the problem? He points out in several cases the Navy has been reduced from an apparent position of choice to a single selection of equipments because of inadequate considerations given to these 9 points by designers and suppliers. He then points out particular criteria in the computer area. These are computer speed, computer memory size, availability of visual displays, physical characteristics such as size, power, and weight, availability of high-speed printers, and a degree of standardization which is feasible. The article is of particular interest to those making proposals for computers to be used by the Department of the Navy.

N. H. Taylor

681.142 58-4

The Principles of Universal Numerical Computers—F. H. Raymond (*Onde élect.*, vol. 36, pp. 838–841; October, 1956, and vol. 37, pp. 68–78; January, 1957.) Continuation and conclusion of paper included in the Electronic Computer issue of the journal.

Courtesy of Proc. IRE and *Wireless Engineer*

681.142:621.394-3 58-5

Morse-to-Teleprinter Code Converter—W. R. Smith-Vaniz and E. T. Barrett. (*Electronics*, vol. 30, pp. 154–158; July 1, 1957.) An analog-digital computer converting international Morse-code signals into standard five-digit teleprinter code.

Courtesy of Proc. IRE and *Wireless Engineer*

58-6

Evaluation of Transistor Life Data—J. D. Johnson and B. VanSwearingen. (IRE Trans. on Reliability and Quality Control, vol. 11, pp. 15–26; August, 1957.) The purpose of evaluating transistor life data is to make possible proper application, specification, and design of transistors. There are many methods of testing and analyzing life characteristics. These methods are reviewed and discussed here from the standpoint of the user, with emphasis on a particular statistical approach. Components are initially evaluated at different temperatures to determine such general characteristics as current gain and leakage currents in the collector and emitter cutoff region. Samples are also submitted to mechanical and environmental tests. Life tests are conducted at various temperature and power levels. As a control feature, shelf life tests are usually performed simultaneously. Data collected from life tests are recorded on punched cards. Each card contains all the data for a given transistor at a particular time during the life test. This information is used as the input for an electronic calculator by means of which statistical summaries can be computed. The use of calculators accelerates the evaluation period and therefore allows more data to be analyzed efficiently. This method permits either individual or group evaluation procedures. Results are presented on curves and charts.

Courtesy of Proc. IRE

ANALOG EQUIPMENT

681.142:621.383.2 58-7

An Electromagnetic Simulator for a Hill's Equation—J. Valat. (*C. R. Acad. Sci., Paris*, vol. 244, pp. 2462–2465; May 13, 1957.) Description of a system based on a mirror galvanometer and twin-anode photocell with application to the calculation of cosmotron orbits.

Courtesy of Proc. IRE and *Wireless Engineer*

DIGITAL COMPONENT RESEARCH

681.142:621.374.32:621.314.7 58-8

Computer Switching with Micro-alloy Transistors.—J. B. Angell and M. M. Fortini. (*Electronic Ind. Tele-Tech.*, vol. 15, pp. 38–39, 126; December, 1956.) Transistor characteristics are discussed in relation to flip-flop circuits.

Courtesy of Proc. IRE and *Wireless Engineer*

621.318.57:621.314.7 58-9

Boosting Transistor Switching Speed—R. H. Baker. (*Electronics*, vol. 30, pp. 190–193; March 1, 1957.) The advantages of combining *p-n-p* and *n-p-n* transistors and other switching circuit improvements are briefly outlined.

Courtesy of Proc. IRE and *Wireless Engineer*

621.374.32:621.314.7 58-10

High-Reliability Transistorized Counter—H. C. Chisholm. (*Electronics*, vol. 30, pp. 171–173; June 1, 1957.) "Cascaded silicon-junction transistor binary stages energize neon-lamp indicators for digital frequency meter at counting rates up to 100,000 per second."

Courtesy of Proc. IRE and *Wireless Engineer*

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—The Editor

.374.32:621.314.7 58-11
Decade Counters using Junction Transors—L. P. Morgan and W. L. Stephenson. *ullard Tech. Commun.*, vol. 3, pp. 2–10; ruary, 1957.) A practical desigh with a nting speed of 100 kc uses one binary and asymmetrical bistable circuits.

Courtesy of PROC. IRE and *Wireless Engineer*

.142:621.314.7 58-12
Computer Delay Unit Uses Semiconors—W. A. Scism. (*Electronics*, vol. p. 173; July 1, 1957.) Three point-con-transistor multivibrators are cascaded rovide a delay of 40 μsec per stage.

Courtesy of PROC. IRE and *Wireless Engineer*

.373.431.1:621.387.4 58-13
Experimental Investigations of the Dead e of Univibrators—D. Kiss and J. ek. (*J. Sci. Instr.*, vol. 34, pp. 99–100; rch, 1957.) The earliest time in which a nostable multivibrator can be triggered r a previous triggering is found to be ngly dependent on the amplitude of the gering pulse.

Courtesy of PROC. IRE and *Wireless Engineer*

.226/.227:546.431.824–31:681.142 58-14
Barium Titanate and its Use as a Mem Store—D. S. Campbell. (*J. Brit. IRE*, 17, pp. 385–395; July, 1957.) A practical K10 unit can be constructed in a square . Properties of the material limit the imum access time to 10 μsec, but tranor drive circuits can be used since large ents are not required.

Courtesy of PROC. IRE and *Wireless Engineer*

.142 58-15
Magnetic Data Recording Theory: Head ign—A. S. Hoagland. (*Commun. and tronics*, no. 27, pp. 506–512; November, 6.) The relation of the read-back wavein to bit density is examined and basic oretical expressions are derived. The gn of a recording head for magnetic s is discussed with the aid of experital results.

Courtesy of PROC. IRE and *Wireless Engineer*

58-16
A Technique for Using Memory Cores Logical Elements—L. J. Andrews. (*Proc. ttern Joint Comp. Conf.*, December 10–12, 6, N. Y., pp. 39–46; 1957.) The regular hysteresis loop of small ferrite mory cores is used to obtain a gating or tching action. A core is excited with a gnetomotive force of $-H_{m/2}$ for each aal function, (proposition), that it is at the given time, at the same time that core is excited with $+H_m$ from a clock rce. The magnitude of H_m is chosen such t it will switch the core while $H_{m/2}$ will switch the core. Thus the presence of of the signals will inhibit the switching on of the clock. This element is a er complementer. Quite complex strucs can be constructed by suitable interinection of this elementary logical elent. The signal windings, clock windings, sense windings of a number of cores are nected in series to build up the more complex circuits. Register, flip-flops, and a small complete machine are described. The outputs of the core circuits are fed into transistors which provide power gain and in turn drive other core circuits. The explanations of the basic elements and complex circuits are vague and difficult to follow. The author does not present any details of the transistor circuit which connects various groups of cores. Thus many of the systems considerations can only be imagined. Design considerations are also omitted.

T. H. Bonn

681.142:621.318.57:621.3.042 58-17
The Reading of Magnetic Stores without Loss of Information—A. Darré. (*Frequenz*, vol. 11, pp. 19–27; January, 1957 and pp. 38–42; February, 1957.) A description and comparison of storage and read-out methods using various forms of the "transfluxor" and of toroidal core devices.

Courtesy of PROC. IRE and *Wireless Engineer*

58-18
A Magnetically Controlled Gating Element—D. A. Buck. (*Proc. Eastern Joint Comp. Conf.*, December 10–12, 1956, N. Y., pp. 47–50; 1957.) Magnetic destruction of superconductivity is the principle of a new computer element called "cryotron." It is based on the nonlinear relation between resistance and magnetic fields at very low temperatures known as "quenching effect." The actual circuit comprises a pair of straight superconductors equipped with single layer control windings. Appropriate feedback connections lead to bistable operation which is particularly suited for certain data processing applications. Presently used cryotrons have switching times in the order of 500 μsec which is a limitation of major significance. The switching time depends on the penetration depth of the quenching effect and is directly related to the minimum thickness of the superconductor. As soon as superconductors can be produced in very thin layers the transition or switching time will be shortened considerably and then a wider application of cryotron may be expected.

Ernest J. Schubert

621.318.57:621.387 58-19
Counters and Control Circuits with Coincidence Thyratrons—L. Hartmuth. (*Nachr. Tech. Z.*, vol. 10, pp. 141–144; March, 1957.) The application of the thyratron Type ST80T is briefly discussed.

Courtesy of PROC. IRE and *Wireless Engineer*

58-20
Final Report, Second Series—J. R. Bowman, F. A. Schwertz, *et al.* (*Computer Components Fellowship Mellon Inst.*, i+40 pp.+49 figures+appendix; October 1, 1953 through September 30, 1956.) The report is a triennial summary of a research program in which new devices suitable for use in digital computing machinery and other data processors were sought. At the beginning of the period emphasis was on investigations of physical phenomena for component applications. Work on nonlinear resistors resulted in adder circuits formed by printing conducting circles on opposite sides of bonded sheets of silicon carbide grain. The circles were connected by printed conducting lines into matrices. Saturable transformers were used in the construction of gating circuits. A hard vacuum tube was made with a photocathode and a phosphor-anode which was bistable and was triggered by light pulses. Preliminary experiments were conducted to produce electro-optical transducers and switches. The phenomenon of electroluminescence was investigated in some detail. Later in the program emphasis was shifted to the fabrication of modular printed circuits capable of continuous service in the temperature range of −60° to +200°C. Various techniques were developed to fabricate on a single substrate such passive components as conductors, capacitors, inductors, and resistors. These include the use of Xerography, vacuum evaporation deposition, chemical decomposition, and the screen process for the formation of resistance, dielectric, and conductive films on a desired substrate surface.

C. H. T. Wilkins

DIGITAL SYSTEM RESEARCH

681.142 58-21
Number Systems for Computers—J. J. Gabelman. (*Electronic Ind. Tele-Tech.* vol. 15, pp. 32–33, 118; December, 1956.) Decimal, binary, octal, biquinary, coded decimal, and excess-three systems are considered.

Courtesy of PROC. IRE and *Wireless Engineer*

681.142:511 58-22
A System of Mathematical Symbols Suitable for Calculations by [digital] Computers—L. V. Kantorovich. (*C. R. Acad. Sci. U.R.S.S.*, vol. 113, pp. 738–741; April 1, 1957. In Russian.)

Courtesy of PROC. IRE and *Wireless Engineer*

621.318.5:[681.142+621.316.7 58-23
A Method of Synthesis of Computing and Control Switching Circuits—G. N. Povarov. (*Avtomatika i Telemekhanika*, vol. 18, pp. 145–162; February, 1957.) The method described is applicable to bridge-type multiple switching circuits, and particularly to symmetrical circuits. Illustrative examples are given.

Courtesy of PROC. IRE and *Wireless Engineer*

58-24
Logical Design of the Digital Computer for the SAGE System—M. M. Astrahan, B. Housman, J. F. Jacobs, R. P. Mayer, and W. H. Thomas. (*IBM J. Res. and Dev.*, vol. 1, pp. 76–83; 1957.) This paper describes what is probably the largest, fastest, and most expensive automatic stored program digital computer in operation, at least in the United States. Designed for application to the SAGE air defense system, it is actually a general-purpose digital computer with specialized features. Its high-speed magnetic core storage contains 8192 words, each of 32-bits plus parity digit. Approximately 100,000 words of auxiliary drum storage are also provided, with five magnetic tape units and a cathode ray tube display system. The computer is almost completely duplexed for the purpose of reliability. Its multiplication

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ed for 16-bit numbers is 17.5 μsec, prob- the limit for the class of circuitry in- ved. It also contains a standard indexing "*B*-Line" system; unfortunately the hors have not credited Williams or ing of Manchester, or the designers of MIDAC and Datatron in the U.S.A., had priority with this technique. Input- put allows simultaneous operation and a-handling through buffer-storage drums. the mathematician, the following are ortant: 1) This is the first computer to form multidimensional operations (arith- ic on two-dimensional vectors); 2) the eduling problem for computers employ- such concurrent operation is acute; ch further analysis will be needed; 3) this nputer, of which many copies will be le, has not been planned so that upon military obsolescence, it could be of use to niversity or other research organization lire need of computation facilities; and the extremely complex logical problem uired in the "programming" of problems such equipment is well worth sincere thematical investigation.

John W. Carr, III
Courtesy of *Mathematical Reviews*

58-25

A Cryotron Catalog Memory System—E. Slade and H. O. McMahon. (*Proc. stern Joint Comp. Conf.*, December 10–12, 6, N. Y., pp. 115–119; 1957.) This cle describes several potentially useful blications and circuit configurations for A. Buck's cryotron, a device which relies the magnetic destruction of supercon- tivity. Slade and McMahon describe a ary decoding switch, which uses several bium coils on each tantalum gate and ch is considerably easier to construct n the same circuit composed of elemen- y single coil cryotrons. In addition, a otron flip-flop is described, complete h input and output gates. The authors lly describe a cryotron catalog memory tem which uses the two circuits men- ed above in addition to an extremely in- sting bridge-type interrogation device. errogation in this memory system is un- ventional in that it consists of determin- whether or not a specified word is in the mory. A four-word memory with each rd consisting of five bits has been built, l a 40-word memory is under construc- n. The authors estimate the write opera- n will require 500 μsec and the interrogate, μsec.

R. C. Minnick

DIGITAL EQUIPMENT

1.142 58-26

The "Metrovick 950" Digital Computer R. M. Foulkes. (*Metropolitan Vickers z.*, vol. 28, pp. 111–117; May, 1957.) The nputer is a medium-speed general-pur- se binary machine designed for applica- n to mathematical and scientific prob- ns. The first model was completed in July, 56. Transistors are used in the computing cuits and thermionic tubes in the circuits writing on the magnetic storage drum. e method of operation of the transistors that described by Chaplin.

Courtesy of Proc. IRE
and *Wireless Engineer*

681.142 58-27

LACE (The Luton Automatic Computing Engine) Part 1—R. J. Gomperts and D. W. Righton. (*Electronic Eng.*, vol. 29, pp. 306–312; July, and 380–385; August, 1957.) The general-purpose analog computer in operation at the Guided Weapons Division of the English Electric Company was designed to have a high utilization and growth factor. Four separate units called "bricks" are available which may be operated in combination or separately. **Part 2**—J. C. Jones and D. Readshaw. A description of 1) an electronic multiplier and 2) an electronic general-purpose function generator developed for use with LACE.

Courtesy of Proc. IRE
and *Wireless Engineer*

681.142 58-28

The Development of a Business Computer System—A. S. Johnston and S. L. H. Clarke. (*J. Brit. IRE*, vol. 17, pp. 351–364; July, 1957.) Describes the Elliott 405 system, incorporating a 1.6-m nickel delay line and a new type of store using 35-mm film coated with magnetic oxide.

Courtesy of Proc. IRE
and *Wireless Engineer*

58-29

Univac-Larc, the Next Step in Computer Design—J. P. Eckert. (*Proc. Eastern Joint Comp. Conf.*, December 10–12, 1956, N. Y., pp. 16–19; 1957.) This paper describes the plans for the Livermore Atomic Research Computer which is being built by the Remington Rand Univac Division. The Computer is scheduled for delivery in 1958 to the University of California Radiation Laboratories, Livermore, Calif. The paper describes the systems techniques which will allow an increase in calculation rate of more than 100 times over present scientific computers, with a pulse rate of only 2 mc. The Larc will have parallel decimal arithmetic, both fixed and floating point, complete checking, multiple arithmetic and index registers, and simultaneous input/output and computing. There will be separate processors for arithmetic operations and for input/output control and processing. Each of these computers will have overlap operation for handling instructions, index registers, and operands. Provision will be made for adding a second arithmetic computer. The planned use of automatic programming allows the provision of a very large and complex order code for more efficient processing. The memory system consists of 1-μsec A and B registers; multiple 4-μsec core memories of 25,000 words each; multiple 250,000-word drums; and magnetic tapes. The multiple memory units may be used simultaneously. Some planned operation speeds are 4 μsec for floating or fixed decimal addition and 8 μsec for floating rounded multiplication. The paper describes these and other features in a quite general manner, stating that a detailed presentation is beyond the scope of this paper.

M. M. Astrahan

58-30

Datafile—A New Tool for Extensive File Storage—D. N. MacDonald. (*Proc. Eastern Joint Comp. Conf.*, December 10–12, 1956, N. Y., pp. 124–127; 1957.) The design of the Datafile is described briefly with a discussion of capacity-access time relations with respect to file applications. The machine has 50 tapes, each 250 feet in length, stored in a partitioned tub. A servo-positioned head carriage services the selected tape for recording operations. Total capacity is 22 million decimal digits with an average random access time of 14 seconds. Since the Datafile is a quasi-random access unit, file organization and its influence on system efficiency is touched upon.

A. S. Hoagland

681.142 58-31

Typed Figures Translated into Computer Code: High-Speed Reading by Electric Automaton—(*Engineering, London*, vol. 183, pp. 348–349; March 15, 1957.) Description of a pilot model of the electronic reading automaton (ERA). A flying-spot scanning system provides 100 bits for the recognition of each typed figure. The use of many redundant bits ensures that minor defects in typescript do not affect the accuracy of the information supplied to the computer.

Courtesy of Proc. IRE
and *Wireless Engineer*

681.142 58-32

Digital Printer Boosts Readout Time—H. W. Gettings. (*Electronics*, vol. 30, pp. 182–185; June 1, 1957.) The system can print 180 lines of 12 characters per line in 1 second.

Courtesy of Proc. IRE
and *Wireless Engineer*

58-33

The Burroughs Electrographic Printer-Plotter for Ordnance Computing—H. Epstein and P. Kintner. (*Proc. Eastern Joint Computer Conf.*, December 10–12, 1956, N. Y., pp. 73–80; 1957.) By combining techniques drawn from facsimile and xerography and by forming an "image" of what is to be printed within the memory of the computer, a new type of output mechanism for high-speed computers is developed. The device described accomplishes a "line" of printing each 100 msec. The "line" occupies an area of 10 inches by 0.6 inch on the paper and permits expression of arbitrary patterns with a 15,000-dot matrix. As utilized by the authors these dots may express 30 consecutive points of a graphical plot having a resolution of 1/500 or three lines of characters. In the latter form each character is assigned a 5 by 7 dot matrix thus achieving 72 characters across the paper or 216 characters within the matrix. (An allowance of two dots between characters and three dots between lines is made.) The system uses a specially coated paper which is charged at each location where a dot is to be printed during the passage of a 30-point comb across the paper. Thirty pulse generators connect to elements of the comb and are pulsed upon coincidence of an information bit in the computer memory and one of the 500 timing pulses derived from an optical source carried on the scanning wheel. Since the passage of the comb is accomplished in 20 msec, the computer must be capable of supplying 30-bit words each 40 μsec and of preparing a new image in its memory in the intervening 80 msec to maintain the full printing rate. After being

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rged with the desired pattern, the paper nked and fixed in a manner identical to ography; however, the authors prefer the m electrographic. The article is explicit ing several illustrations of printed sam- s and mechanical and circuit details.

John L. Hill

58-34

Mechanization of Post Office Operations—Anonymous. (*NBS Tech. News Bull.*, . 41, pp. 174–176, November, 1957.) er letters have been culled, faced, and celled, an operator reads the address and, ough a keyboard, imprints on the en- ope an abbreviated address coded in chine-readable dots of fluorescent ink. rting is then mechanized by translators t tell distributors into which output bin drop the letter. A translator requires an ensive built-in memory of the delivery te structure. This is contained in a stack perforated metal cards. Access is obtained displacing selected cards and output is ived by observing the locations at which nt shines through the stack.

R. D. Elbourn

UTILIZATION OF DIGITAL EQUIPMENT

58-35

Proceedings of the Second Annual Computer Applications Symposium, October 24–25, 1955. (Sponsored by Armour Res. und., Ill. Inst. Tech., Chicago, Ill., 108 ; 1956.) This is a collection of reports of ks delivered at the symposium, together h the discussion which followed each er. For all practical purposes, the word gital" could be in the title of the sym- ium. The program was devoted to seven pers having to do with "Computers for siness and management," and seven con- ned with "Computers for engineering d research." Twelve papers and one ab- act appear in the *Proceedings*, as follows: *mputers for Business and Management:* he use of digital computers in industry," R. F. Clippinger; "A dollar and cents proach to electronics," by John L. Marley; n application of computers to general okkeeping," by W. F. Otterstrom; "User periences and applications of the ERA 03," by George E. Clark; "Automobile ective underwriting and automatic rating the IBM 650," by C. A. Marquardt; utting costs with linear programming," Jacob E. Bearman; "Probability fore- sts in management decisions (abstract)," Stanley Reiter. *Computers for Engineer- and Research:* "Use of the IBM 650 in entific computations," by A. W. Wymore; ngineering applications of large scale nputers," by C. B. Ludwig; "High speed mputation of engine performance," by T. Horner; "Pyrolysis reactor design com- tations," by H. C. Schutt and R. H. ow; "Aircraft flight test data processing," T. M. Beilan; "Programming a Monte rlo problem," by J. F. Hall and J. M. ok. The *Proceedings* contain some infor- tion which is very useful for those inter- ed in the two broad fields covered.

T. H. Southard

Courtesy of *Mathematical Tables and Other Aids to Computation*

681.142 58-36

Electronic Computer Study of English Syntax Patterns—(*NBS Tech. News Bull.*, vol. 41, pp. 84–86; June, 1957.) Report of an exploratory study for data-processing purposes.

Courtesy of PROC. IRE and *Wireless Engineer*

681.142:519.283 58-37

The Generation of Random Numbers on Automatic Computers—S. von Hoerner. (*Z. angew. Math. Phys.*, vol. 8, pp. 26–52; January 25, 1957.) Some mathematical methods are summarized and a new one, which avoids the formation of stable cycles and degeneration, is discussed. The theory of random-number generation using γ radiation is confirmed by means of the experimental arrangement described.

Courtesy of PROC. IRE and *Wireless Engineer*

681.142:681.176 58-38

Computer Selects Premium Bond Winners—R. K. Hayward, E. L. Bubb, and H. W. Fensom. (*Electronics*, vol. 30, pp. 138–143; July 1, 1957.) A description of the electronic random number indicating equipment (ERNIE) used to print a list of purely random bond numbers. (See also Hayward and Bubb, *P. O. Elec. Eng. J.*, vol. 50, pp. 1–6; April, 1957.)

Courtesy of PROC. IRE and *Wireless Engineer*

58-39

Wage Accounting by Electronic Computer—National Physical Laboratory. (Report No. 1, Inter-Departmental Study Group on the Application of Computer Techniques to Clerical Work. Her Majesty's Stationery Office, London, 57 pp.; 1956.) This 57-page booklet reports on one of the earliest applications of computers to commercial work in England; the application is a government payroll calculation, and the machine used is the DEUCE. The report is quite complete, including block diagrams, time and cost data, and even considerable discussion of computers *per se*, reliability, and a section on data sorting. Following are some of the report's conclusions: 1) A "scientific computer" with magnetic tape input-output forms an adequate machine for payroll work. 2) The reliability of this operation is satisfactory if attention is given to program checks, proper machine maintenance, and safety margins in the time schedule; automatic "built-in" checking is not essential. 3) The computer permits reduction in clerical staff, but further economies could be obtained if input data were originally recorded in appropriate form. 4) The report contains cautious statements indicating that payroll work may justify or at least help justify a computer installation in many organizations. The DEUCE (successor to ACE) has a 250,000 bit magnetic drum, 32-bit word size, mercury delay line high-speed store, and 2-msec multiply time.

D. D. Wall

Courtesy of *Mathematical Tables and Other Aids to Computation*

58-40

Generation and Use of Orthogonal Polynomials for Data-Fitting with a Digital Computer—George Forsythe. (*J. Soc. Ind. Appl. Math.*, vol. 5, pp. 74–88; June, 1957.) This paper develops the theory and practice of data-fitting according to the criterion that the sum of the squares of the residuals is to be minimized. As the author states, this note is a self-contained presentation of material on the subject; because of this, the paper is a valuable contribution.

Thomas H. Southard

BOOK REVIEWS

58-41

Mathematics and Computers—George R. Stibitz and Jules A. Larrivee. (McGraw-Hill Book Co., Inc., New York, N. Y., vi+228 pp.; 1957.) The eleven chapters of this book cover nearly all phases of digital computer design and use. The first three chapters cover the basic elements of computers and mathematics, such as the basic differences between the analog and digital computers and the mathematical definition of a function. These early chapters also include some of the history of mathematics and computing, and outline the types of problems arising in applied mathematics which can be and are solved by computing techniques. The fourth chapter is a discussion of the history of computers which is both interesting and informative but, unfortunately, does not go beyond the ENIAC computer to a description and discussion of the more recent history of stored program computers. The fifth chapter contains discussions of some numerical techniques including those for finding roots of polynomials, solving linear equations, and solving ordinary and partial differential equations. This chapter gives an excellent insight to the beginning student on some of the techniques, but many of the techniques presented are not practical for the modern electronic computer. Bernoulli's method for finding roots of a polynomial equation, for example, is of little importance in the modern computing world. The next three chapters discuss digital computer components, number systems, computer memories, and analog-digital converters. These chapters also outline techniques for performing arithmetic processes in the digital computer, and contain an elementary description of how the computer carries out its operations on the basis of a stored program. The analog computer is likewise treated in these chapters, and the techniques for the mechanical differential analyzer in performing integration are explained. Chapter 9 is a discussion of Monte Carlo techniques and includes an explanation of the solution of linear equations by these techniques. The discussion on sampling techniques includes brief discussions on the solution of certain certain partial differential equations and techniques for generating "random" sequences. Chapter 10 is a discussion on the various errors which can occur in both analog and digital computers. Chapter 11 summarizes various special-purpose applications of computers such as those seen in the automatic factory, language translation, and, in a lighter vein, computers which play

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—*The Editor*

es. The central difficulty of this reviewer valuating this book is in deciding to m the information is directed. The book ns to be too elementary to serve as a rence book for any computer profes- al, either user or designer. On the other d, the book does not go into sufficient il in any area to be a successful textbook most university courses. It could, how- , serve as a textbook on an introduction omputers given to freshman or sopho- e students or more advanced nonscience dents. It could also serve as a reference the beginner in the field or for a non- essional. The most serious shortcoming he book is that the material is not suffi- tly modern. Many of the numerical niques presented are old-fashioned and damentals are often described in terms old-fashioned equipment rather than dern equipment. (An analog-digital con- er could be easily described in terms of ing and comparing the voltage rather n in terms of the mechanical device ch transmits a shaft position to a me- nical digit position.) The authors leave false impression that tables, especially se involving the elementary functions, are uently stored in computer memory. Of- modern words are not used; for example, words "subroutine," "programmer," and term "parity check bit," are not used in ribing and discussing these items. The e of the book is light and enjoyable and es interesting reading. The bibliography od and extensive.

Walter F. Bauer
Courtesy of *Mathematical Tables and Other Aids to Computation*

58-42

Faster, Faster—W. J. Eckert and Re- a Jones. (McGraw-Hill Book Co., Inc., York, N. Y., vii+160 pp.; 1955.) ting from the preface, "This monograph n attempt to explain in nontechnical lan- ge how a calculator operates, the nature he problems it solves, and how the prob- s are presented to the calculator." ually, it consists almost entirely of a cription of "NORC," the Naval Ord- ce Research Calculator designed and built the International Business Machines poration. Probably only a few experts uld agree to the claim that NORC . is also easiest to understand" (preface) the explanatory attempt must be judged y successful; it is completely devoid of ineering details (such as component es, circuit diagrams, etc.), relying in- ad upon simple block diagrams and ematics accompanied by descriptions of essential properties involved. The lan- ge is indeed nontechnical, even such mon descriptive contractions as "and/or e" being avoided, although various col- uialisms native to business machinery, h as "echo-pulse," "print cycle," are ex- ined and used. Here and there the view- nt tends to be a bit insular; for instance basic electronic building block turns to be a binary pulse shaper producing 1- c time delay; this is called a Dynamic se circuit, written always with capitals, a Thing. Again, no allusion is made to except IBM equipment, nor to technical tributions by any outsiders except F. C. Williams, the Red Queen, Leibniz and Newton. Chapter I is introductory, and begins with a general outline of the need for, and requirements of automatic *en masse* arithmetic, and sketches the typical mental, organizational, and instrumental hurdles that must be overcome. Lucid examples of basic arithmetical and scaling operations are given, as well as various notions about electronic components, timing relationships and the role of main functional units such as the arithmetical, memory, input-output, etc. Halfway through the chapter all such generality is jettisoned without rites and supplanted by a clear outline of NORC's code-language, organization, structure, and philosophy; these and other features of NORC are more fully developed in all chapters but the last of the ten that follow, and in five summarizing appendices. The level of exposition is, on the whole, excellent; one may take exception—as does this reviewer—to the practice of attaching grammatical commas and periods to arithmetical examples, and to the use of the word "accuracy" instead of the word "reliability" in contexts where freedom from accidental errors is meant, but aside from these trivialities of taste, the exposition leaves little to be desired. NORC is revealed to be quite a fast machine (70 μsec to multiply; 50 to add or subtract; 250 to divide; 8 for memory access), with ample memory capacity (3600 words, each 66 bits) composed of 4 banks of Williams crt storage, supplemented by 8 magnetic tape units of impressive capacity (400,000 words each) and speed (4000 words/second), plus printing (19 words/second) and card punch/read facilities (400 words/minute). Each order is an instruction plus three addresses, the latter automatically modifiable en route. The instruction list is almost lavishly flexible; all standard arithmetic operations are available with options of floating point (± 30), automatic sizing shifts, extractions for order modification, transplantation of addressees, etc. There are no less than 21 control transfer instructions, plus 5 for print control and 9 for tape control; the grand total is 98. Data entries are normally preserved to 13 decimal places, and there appears to be an efficient provision for double-precision arithmetic. Beyond doubt, NORC should be classed as an outstandingly flexible and effective computing system. Electronically, NORC belongs in the category of "pulse recirculating" machines typified by SEAC of the National Bureau of Standards. These machines avoid the use of static memory cells of Eccles-Jordan "flip-flop" type in their arithmetical and logical units by routing binary pulses through various circulating paths consisting of time delay and pulse re-shaping components. Since identification of pulse position in this moving coordinate system is vital, a central clock is used to quantize the time coordinate and great stress is laid upon matters of timing, pulse shaping, and synchronism. The internal language of NORC consists of words $16\frac{2}{3}$ decimal digits long, each digit being represented by a tetrad of binary digits. It is actually true that arithmetic within the machine is carried out in this mixed base, elements of an essentially binary nature (aggregates of dynamic pulse units plus gangswitches) being combined so as to preserve the local identity (*i.e.*, within tetrads of wires, elements, etc.) of decimal characters. Words are taken from or put into the memory as 66-bit parallel transfers, within the arithmetic unit the basic process involves 4-abreast shifting of successive tetrads to effect, for instance, addition that is decimally serial. Multiplication is done by a similar shift of the multiplicand stepwise through a parallel circuit called a "product generator" equivalent to a multiplication table, so that as each multiplicand digit steps up to the altar, all ten multiples of it become simultaneously available. From this array all multiples specified by the multiplier digits can thus be accumulated at each multiplicand step, and the entire product assembled during one "pass." Consequently multiplication is almost as brief as addition, though division does not fare comparably well, requiring four or five times as long. A little bookkeeping may suggest that NORC is somewhat extravagant with regard to information capacity, one binary tetrad capable of representing 16 alternatives being used to represent only 10, etc. This glaring redundance is the decimal man's burden and seems unavoidable; in NORC some slight byproduct utility is recovered by using "12" and "13" for magnetic tape word-end and block-end signals. Much emphasis is placed upon automatic checking throughout the discussion and NORC uses two systems, 1) modulo 4 summing of the bits in each word, affixing half a tetrad of redundance to tag this, and 2) "casting-out-nines" checking of the arithmetic operations. Together 1) and 2) seem to make good sense, whereas 1) alone would be quite weak since repeated doublings play a key role in the product generator. In the Williams memory a parity check is also provided for the sum of the bits in each of the 66 parallel positions. Altogether, these features inspire confidence, yet in a machine having some one-third of its capacity redundant, one wonders whether it might not have been feasible to make the checking density far more severe. The reader concerned with machine design will appreciate that NORC has been moulded to fit rigorously within a framework of precepts: decimal, speedy, ample capacity, big vocabulary, pulsed circuits, checking. Probably not everybody would choose exactly this prescription, but few would deny that it is interesting and bold, and seems to have been carried out with systematic skill and generous material resources, and with the sort of opportunistic ingenuity that is the hallmark of elegant design. The field of computer design is advancing so rapidly both in technology and in concepts that no design group can claim ultimate insight, and all may well benefit from a study of the various species evolved. NORC deserves careful study, and it is to be hoped that a careful comparative examination of its operational performance will eventually be published. The final chapter in "Faster, Faster" is entitled, "What is There to Calculate?" and consists of a very elementary but clear discussion of calculations applied to linear systems, ballistic trajectories, planetary motion, etc. Perhaps a slight improvement could be made by distinguishing more carefully the idea of solving a mathematical problem in general from

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idea of calculating a numerical solution; page 131 following a discussion of bal- cs, the statement that "A slightly more plicated problem is the three-body blem" may illustrate this point. Aside n this, the discussion of numerical pro- ures is well suited to convey the flavor his field to the nonspecialist.

J. H. Bigelow

Courtesy of *Mathematical Tables and Other Aids to Computation*

58-43

The Office in Transition—Esther R. ker and Eugene F. Murphy. (Harper and thers, New York, N. Y., x+190 pp.; 7.) This book discusses the changes ng place in offices today as a result of introduction into the business world of puters and auxiliary equipment, with r accompanying improved techniques he handling of information. It is, accord- to the authors, intended for adminis- ors in business who wish to investigate mation to see if it could be used to ad- tage in their offices. It is further intended elp them to select the proper degree of hanization (as the authors sensibly nt out that large-scale computers would waste for businesses whose volume of e work did not justify their expense), ise new systems for better results, and dle any attendant personnel problems sfactorily. The authors also state that it ntended for people in education as a text t can be "integrated into the Business ministration curriculum," and for those king a philosophy of automation in the e, in simple terms that can be under- d by those not in the business world." an introduction to the subject, it ful- its purpose well, for the book is written very elementary level, with the authors arently assuming that the reader is hav- his first introduction to both computers office automation. A great deal of space evoted to methods of handling and pre- ting personnel problems that might arise ause of the change in types of jobs in the e due to automation. The book contains endices on: 1) Equipment Descriptions, Manufacturers of Business Machines and uipment for the Automatic Office, and 3) sociations, Institutions, and Publications ich includes a list of colleges and uni- sities offering courses in machine ac- nting, business use of punched card or a processing machines, and related sub- ts).

V. R. Huskey

58-44

Electronic Data Processing for Business d Industry—R. G. Canning. (John Wiley d Sons, New York, N. Y., xi+332 pp.; 6.) Canning's book describes electronic a processing as a new management tool. tterns of data processing are given with rticular attention being paid to inventory trol and to shop scheduling. Program- ng of typical operations is briefly de- ibed. Various systems of data processing considered. Differences between general rpose computers and special purpose data cessing equipment (such as sorters and maintenance devices) as well as the general characteristics of such devices are given. The last chapter is entitled "Management's Program for Obtaining a Reliable System." Looking at the book from the viewpoint of management the reviewer believes that the greatest criticism of the book concerns the number of times that nonexisting equipment is described. On the other hand, in a field essentially five years old the interval between manuscript and publication is such that the author may need to resort to such devices. This book fulfills a need in assisting management to plan in a fast developing field.

H. D. Huskey

58-45

The Punched Card Annual—(The Punched Card Publishing Co., Detroit, Mich., vol. 2, 208 pp., 1953–54; vol. 3, 232 pp., 1954–55; vol. 4, 200 pp., 1955–56; vol. 5, 208 pp., 1956–57.) These are paper back periodical-type books printed in a two-column format. Volume 2 contains 55 articles on various aspects of machine accounting. These articles account for about 175 pages. A special features section has 30 articles on some 25 pages divided between "Tips on Tabulating" and "Tips on Forms." A few articles are written by staff members of companies selling machine accounting equipment, but most articles are prepared by supervisors of computing or tabulating laboratories. Volume 3 has 48 articles on business applications of punched card equipment. Various accounting procedures make up the subject matter of most of the articles. A "Procedures Exchange Directory" is included. This gives a list of individuals who have volunteered to exchange procedure information. Listings are by type of business and type of procedure. Volume 4 has 59 articles on machine accounting techniques. Volume 5 is divided into two sections, "Management" and "Applications." There are 47 articles on machine accounting and data processing. Six of the articles mention electronic equipment in the titles. There are the usual "Tips on Tabulating." Each volume contains a cross index of itself and the previous volumes.

H. D. Huskey

58-46

Pulse Techniques—S. Moskowitz and J. Racker. (Prentice-Hall, Inc., Englewood Cliffs, N. J., viii+300 pp.; 1951.) The book starts with a discussion of characteristics of pulses. Transient response of linear networks is treated making use of Laplace transforms. Filters, transformers, and delay lines are covered in a discussion of pulse networks. Linear pulse amplifiers, pulse shaping and clamp circuits, and pulse regeneration are considered next. The last three chapters cover pulse measurements and instruments, pulse communication systems, and antenna navigation aids. Three appendices review complex variable theory and discuss the pulse response of cascaded wave filters and transmission lines. Although this is an older book and the examples are in terms of vacuum tube circuits it is a good presentation of pulse circuits as used in digital computers.

H. D. Huskey

58-47

Transistor Circuit Engineering—R. F. Shea, ed. (John Wiley and Sons, Inc., New York, N. Y., xx+468 pp.; 1957.) This book was written by members of the General Electric staff; eight co-authors collaborated with the editor with the objective of combining "a proper mixture of basic transistor theory with examples of its proper application in typical circuits." The chapter headings are: 1) "Characteristics and Characteristic Curves," 2) "Equivalent Circuits," 3) "Bias and Its Stabilization," 4) "Audio Amplifiers," 5) "D-C Amplifiers and Their Applications," 6) "Tuned Amplifiers," 7) "Video Amplifiers," 8) "Oscillators," 9) "Modulation, Mixing, and Detection," 10) "Transient Response and Pulse Circuits," 11) "Systems," 12) "Special Circuits." The book terminates with an appendix on Matrix Algebra of Two-Port Devices and a fourteen page bibliography. Considerable attention is paid to bias stabilization. The book is prolifically illustrated with figures. Equivalent circuits and design formulas are supplied for typical transistor circuitry.

H. D. Huskey

58-48

Transistors Handbook—W. D. Bevitt. (Prentice-Hall, Englewood Cliffs, N. J., xiv+410 pp.; 1956.) Chapter one discusses the historical aspects of transistors and indicates the great expectations held for the device. Chapter two gives fundamental definitions and concepts, chapter three considers point-contact transistors, chapter four, junction transistors, and chapter five, power transistors. Chapters six and seven discuss measurements of transistor characteristics and methods of analysis of transistors and transistor circuits. Chapter eight is on multi-electrode transistors while chapter nine considers photodiodes and phototransistors. Chapter ten covers care of transistors and stabilization of operating points; chapter eleven considers noise and temperature effects. Chapter twelve is on audio and power amplifiers, thirteen is on radio-frequency amplifiers, fourteen and fifteen are on audio and on radio-frequency oscillators. There are two chapters on amplitude and frequency modulation and detection. This is followed by a discussion of radio and television receivers. Relaxation oscillators have a chapter to themselves, followed by a chapter on computer applications of transistors. The last chapter covers miscellaneous applications of transistors. As the author indicates there is no attempt to cover the physical theory of transistors electronics, or to study the design of transistors. Circuit diagrams are given for many applications of transistors.

H. D. Huskey

58-49

Transistor Electronics—A. W. Lo, R. O. Endres, J. Zawels, F. D. Waldhauer, and C. Cheng. (Prentice-Hall, Englewood Cliffs, N. J., xii+521 pp.; 1955.) This book covers the following topics: a qualitative treatment of transistor physics, operating characteristics and parameters, equivalent circuits, basic amplifier configurations, stabilization of dc operating points, low- and high-frequency amplifiers, oscillators, modulation

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—*The Editor*

demodulation, and pulse circuits. Ac-ing to the authors the book is written for vanced undergraduate or graduate stu-s in electrical engineering and associ-fields, and as a reference work for the tronics engineer." Most chapters contain mber of exercises for the student.

H. D. Huskey

58-50

The Law of Inventing in Employment—. Costa. (Central Book Company, New k, N. Y., xiv+336 pp.; 1953.) With the elopment of our economy to the point re the individual rarely has both the nt and the financial background to nt, develop, manufacture, and sell a ce, it is very important for the engineer management to understand fully the tion of the employee-inventor. This k, which is based on the author's dis-ation at the George Washington Univer-School of Law, is a synthesis of Ameri-judicial doctrine bearing on the relation-ship between employee and employer with respect to employee inventions. A chapter of the book covers the basic requirements, scope, nature, and termination of shop rights. The next chapter discusses "inventorship." Third party rights and contract rights form two chapters. Private management and government administration are discussed. Appendices cover 1) Cases—occupations of inventing employees, 2) Government Patents Board, 3) proposed government incentives, 4) patent policies for employees, and 5) an employee suggestion system for the small plant. An extensive bibliography is given and a table of cases mentioned in the text is included. As Dr. Costa indicates, the problem of fair treatment of employer and employee interests has "no imminent across-the-board solution." The recommended course is to educate the employee to his legal rights and to encourage the employer in rewarding employees for inventive contributions. This book serves such an educational purpose.

H. D. Huskey

58-51

Patent Notes for Engineers, 7th Edition—C. D. Tuska. (McGraw-Hill Book Co., Inc., New York, N. Y., vi+192 pp.; 1956.) This book discusses invention in both the popular and technical sense. Requirements of records of inventions are given. Details in the prosecution of applications, interference proceedings, disclosures, and infringements are considered. The book is a must for the individual who is interested in making and patenting inventions. The fact that this book is in its seventh edition further attests to its value. The range of subject matter is indicated by the chapter headings: 1) "Invention in the Popular Sense," 2) "Statutory Invention," 3) "Nature of Statutory Invention," 4) "Statutory Invention as a Practical Matter," 5) "Records of Invention," 6) "Prosecution of Patent Applications," 7) "Interferences," 8) "Patent Approval," and 9) "Ownership and Use of Patents."

H. D. Huskey

INFORMATION FOR AUTHORS

The PGEC TRANSACTIONS is published quarterly and will bear datelines of March, June, September, and December. Abstracts of papers appearing in the TRANSACTIONS will appear also in IRE PROCEEDINGS. The PGEC publication schedule requires about one month for review and correction of all accepted manuscripts. The professional IRE Editorial Staff requires an additional two months' production time from receipt of manuscripts to completion of the printed journal.

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